XPS00000100D116

Cisco® Compatible 10GBase-Converter XENPAK Transceiver (XENPACK to SFP+ Converter, ER)

Product Description

This Cisco® compatible XENPAK to SFP+ converter provides conversion from XENPAK to SFP+ form factors. It is guaranteed to be 100% compatible with the equivalent Cisco® converter. This easy to install, hot swappable converter has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

Features:

- Compatible with XENPAK MSA
- Management and Control Via MDIO 2-Wire Interface
- Hot-Pluggable 70-Pin Connector with XAUI Electrical Interface
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius

Applications:

- XENPAK to SFP+
- Access and Enterprise

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Static Discharge Voltage				500	V	
Data Rate			10		Gbps	

Pin Descriptions

Pin	Symbol	Name/Description	Logic	Notes
1	GND	Electrical Ground.		1
2	GND	Electrical Ground.		1
3	GND	Electrical Ground.		1
4	5.0V	Power Supply of Optical Receiver Frontend.		2
5	3.3V	Power Supply of Optical Receiver and Transmitter and Control Circuits.		2
6	3.3V	Power Supply of Optical Receiver and Transmitter and Control Circuits.		2
7	APS	Adaptive Power Supply. Supply of PHY XS and PCS Layer Devices.		2
8	APS	Adaptive Power Supply. Supply of PHY XS and PCS Layer Devices.		2
9	LASI	Link Alarm Status Interrupt, low active, open drain output. Supposed to operate with 10kΩ to 22kΩ pull upon host. Logic high = normal operation. Logic low = link alarm is indicated.	1.2V CMOS Open Drain Output	
10	Reset	Low active reset input 10kΩ pull-up on transceiver. Logic high = normal operation. Logic low = reset asserted.	1.2V CMOS Input	
11	VENDSPECIFIC	Vendor-Specific Pin for Proper Operation, Leave Unconnected.		5
12	Tx ON/OFF	High active transmitter enable input 10kΩ pull-up on transceiver logic high = transmitter active (normal operation). Register Bit 1.9.0 set to low as well. Logic low = shut down of transceiver.	1.2V CMOS Input	
13	RESERVED	Reserved by MSA, Internally Not Connected.		
14	MOD DETECT	1kΩ to Ground on APS Circuit Environment.		
15	VENDSPECIFIC	Vendor-Specific Pin for Proper Operation, Leave Unconnected.		5
16	VENDSPECIFIC	Vendor-Specific Pin for Proper Operation, Leave Unconnected.		5
17	MDIO	Management Data I/O.		3
18	MDC	Management Clock Input.		3
19	PRTAD4	Port Address Bit 4 (LOW=0), Internally Pulled up to be 18kΩ.	1.2V CMOS Input	
20	PRTAD3	Port Address Bit 3 (LOW=0), Internally Pulled up to be 18kΩ.	1.2V CMOS Input	
21	PRTAD2	Port Address Bit 2 (LOW=0), Internally Pulled up to be 18kΩ.	1.2V CMOS Input	
22	PRTAD1	Port Address Bit 1 (LOW=0), Internally Pulled up to be 18kΩ.	1.2V CMOS Input	
23	PRTAD0	Port Address Bit 0 (LOW=0), Internally Pulled up to be 18kΩ.	1.2V CMOS Input	
24	VENDSPECIFIC	Vendor-Specific Pin for Proper Operation, Leave Unconnected.		5

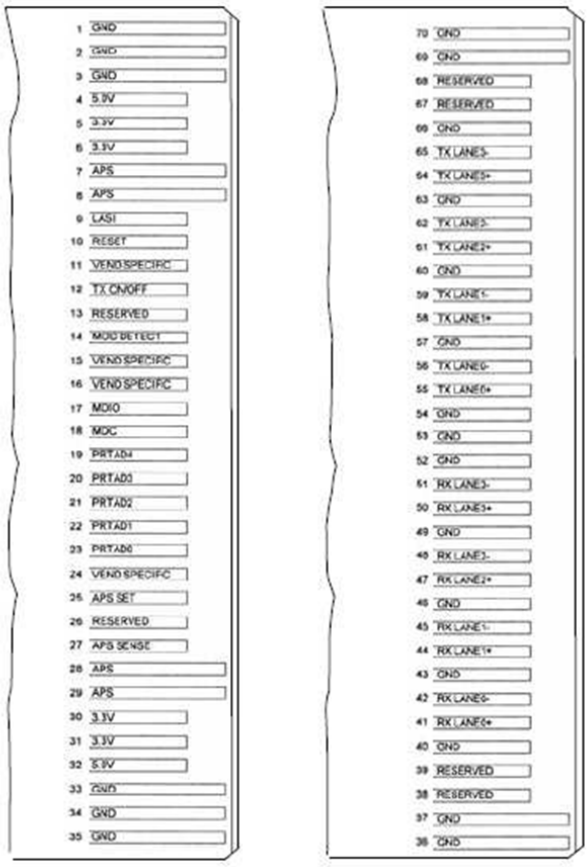
25	APS SET	Feedback Input for APS, Input of APS Setting Resistor.		
26	RESERVED	Reserved for Avalanche Photodiode Use, Internally Not Connected.		5
27	APS SENSE	APS Sense Output for APS Control Circuit.		
28	APS	Adaptive Power Supply. Supply of PHY XS and PCS Layer Devices.		2
29	APS	Adaptive Power Supply. Supply of PHY XS and PCS Layer Devices.		2
30	3.3V	Power Supply of Optical Receiver and Transmitter and Control Circuits.		2
31	3.3V	Power Supply of Optical Receiver and Transmitter and Control Circuits.		2
32	5.0V	Power Supply of Optical Receiver Frontend.		2
33	GND	Electrical Ground.		1
34	GND	Electrical Ground.		1
35	GND	Electrical Ground.		1
36	GND	Electrical Ground.		1
37	GND	Electrical Ground.		1
38	RESERVED	Reserved by MSA, Internally Not Connected.		
39	RESERVED	Reserved by MSA, Internally Not Connected.		
40	GND	Electrical Ground.		1
41	RX LANE 0+	Module XAUI Output Lane 0+.		4
42	RX LANE 0-	Module XAUI Output Lane 0-.		4
43	GND	Electrical Ground.		1
44	RX LANE 1+	Module XAUI Output Lane 1+.		4
45	RX LANE 1-	Module XAUI Output Lane 1-.		4
46	GND	Electrical Ground.		1
47	RX LANE 2+	Module XAUI Output Lane 2+.		4
48	RX LANE 2-	Module XAUI Output Lane 2-.		4
49	GND	Electrical Ground.		1
50	RX LANE 3+	Module XAUI Output Lane 3+.		4
51	RX LANE 3-	Module XAUI Output Lane 3-.		4
52	GND	Electrical Ground.		1
53	GND	Electrical Ground.		1
54	GND	Electrical Ground.		1
55	TX LANE 0+	Module XAUI Input Lane 0+.		4
56	TX LANE 0-	Module XAUI Input Lane 0-.		4
57	GND	Electrical Ground.		1
58	TX LANE 1+	Module XAUI Input Lane 1+.		4
59	TX LANE 1-	Module XAUI Input Lane 1-.		4
60	GND	Electrical Ground.		1

61	TX LANE 2+	Module XAUI Input Lane 2+.		4
62	TX LANE 2-	Module XAUI Input Lane 2-.		4
63	GND	Electrical Ground.		1
64	TX LANE 3+	Module XAUI Input Lane 3+.		4
65	TX LANE 3-	Module XAUI Input Lane 3-.		4
66	GND	Electrical Ground.		1
67	RESERVED	Reserved by MSA, Internally Not Connected.		
68	RESERVED	Reserved by MSA, Internally Not Connected.		
69	GND	Electrical Ground.		1
70	GND	Electrical Ground.		1

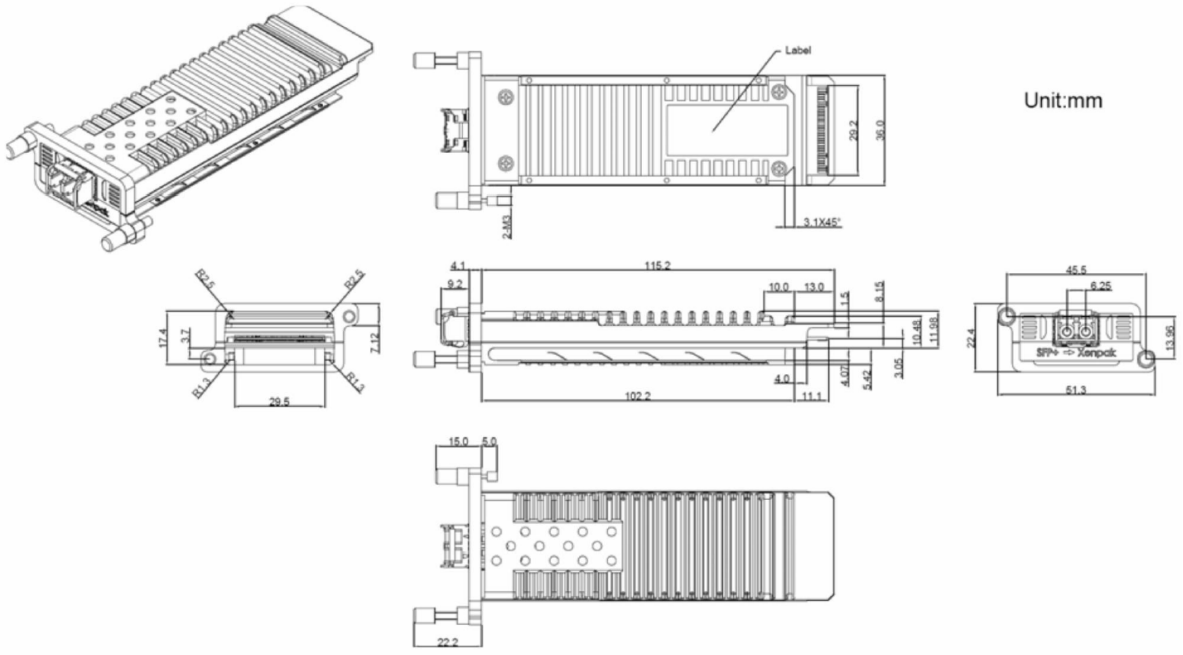
Notes:

1. Ground connections are common for Tx and Rx.
2. Each connector contact is rated at 0.5A.
3. MDIO and MDC timing must comply with IEEE 802.3ae Clause 45.3.
4. XAUI output characteristics comply with IEEE 802.3ae Clause 47.
5. Transceivers will be MSA compliant when no signals are present on the vendor specific pins.

Electrical Pin-Out Details



Mechanical Specifications



About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.