QDD-400G-DCO-ER1-C-SKY

Cisco® Compatible 400GBase-ER1 QSFP-DD Transceiver (SMF, 193.7THz , Coherent, LC, DOM)

Product Description

This Cisco® compatible QSFP-DD transceiver provides 400GBase-Open ER1 throughput up to 50km over single-mode fiber (SMF) using a fixed C-Band wavelength of 1547.72nm via an LC connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Cisco®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

Features:

- QSFP-DD MSA Compliant
- Supports OFEC and CFEC
- Compliant with Open ZR+ MSA and OIF 400ZR MSA
- C-Band 193.7THz Fixed
- Supports Ingress LF Hold-Off Time Configuration
- Client Rate 4x100GbE or 1x400GbE
- Single 3.3V Power Supply
- Duplex LC Connector
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius

Applications:

- 400GBase Ethernet

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	Vcc	-0.3	3.3	3.6	V	Not damaged
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Relative Humidity (Non-Condensing)	RH	5		85	%	
Operating Relative Humidity	RHc	15		85	%	
Receiver Damage Threshold	PRdmg	10			dBm	Total optical power
ESD Sensitivity				1000	V	

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage		Vcc	3.135	3.3	3.465	V	
		Icc			6.9	A	1
Maximum Sustained Peak Current (<500ms)					7.1	A	
Maximum Instantaneous Peak Current (<50us)					8.6	A	
Electro-Static Discharge		ESD			1000	V	
Power Consumption	**400G (400ZR)**	PC		17	18	W	
	400G (400ZR+)			20	21.5		1
Client Mode	**400G (400ZR)**		1 x 400GAUI-8				
	400G (400ZR+)		4 x 400GAUI-2				
Transmission Distance	**400G (OIF 400ZR App Code 0x02)**				40	km	
	400G (400ZR+)				50	km	
Power Supply Noise		Vrip			1%	DC-1MHz	
		Vrip			2%	1-10MHz	

Notes:

1. In 400GbE ZR+ mode, the typical power consumption is 20W, and the maximum power consumption is 21.5W. When switching to 4×100GbE mode, the typical power consumption will be 21W, and the maximum power consumption will be 22.5W. The current will also change accordingly.

High-Speed Electrical Characteristics 400GAUI-8 C2M and 100GAUI-2 C2M

Parameter	Symbol	Min.	Max.	Unit	Notes
Transmitter					
Signaling Rate Per Lane		26.5625 ± 100ppm		GBd	PAM4
AC Common-Mode Output Voltage (RMS)	RMS		17.5	mV	
Differential Voltage Pk-Pk	VIN,pp	750	900	mV	
Near-End ESMW (Eye Symmetry Mask Width)		0.265		UI	
Differential Near-End Eye Height		70		mV	
Far-End ESMW		0.2		UI	
Differential Far-End Eye Height		30		mV	
Far-End Pre-Cursor ISI Ratio		-4.5	2.5	%	
Differential Output Return Loss		Equation (83E-2)			IEEE Std 802.3-2018 Annex 120E
Common- to Differential-Mode Conversion Return Loss		Equation (83E-3)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	At 1MHz
Transition Time (20-80%)	Tr/Tf	9.5		ps	20-80%
DC Common-Mode Voltage	Vcm	-350	2850	mV	
Receiver					
Signaling Rate Per Lane		26.5625 ± 100ppm		GBd	PAM4
Differential Pk-Pk Input Voltage Tolerance	VOUT,pp	900		mV	
Differential Input Return Loss (Minimum)		Equation (83E–5)			IEEE Std 802.3-2018 Annex 120E
Differential- to Common-Mode Input Return Loss (Minimum)		Equation (83E–6)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	
Module Stressed Input Test		See 120E.3.4.1			IEEE Std 802.3-2018 Annex 120E
Single-Ended Voltage Tolerance Range (Minimum)		-0.4	3.3	V	
DC Common-Mode Voltage (Minimum)		-350	2850	mV	

Low-Speed Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
SCL and SDA	VOL	0	0.4	V	1
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Signal	Ci		14	pF	
Total Bus Capacitive Load for SCL and SDA	Cb		100	pF	2
	Cb		200	pF	3
InitMode, ResetL, and ModSelL IntL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	|Iin|		360	uA	0V<VIN<Vcc
	VOL	0	0.4	V	IOL=2.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	10kΩ pull-up to the Host_Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				4

Notes:

1. IOL(max)=3mA for fast-mode, 20mA for fast-mode plus.
2. For 400kHz clock rate, use 3.0kΩ pull-up resistor, maximum. For 1000kHz clock rate, refer to Figure 45 (QSFP-DD-Hardware-rev5p0).
3. For 400kHz clock rate, use 1.6kΩ pull-up resistor, maximum. For 1000kHz clock rate, refer to Figure 45 (QSFP-DD-Hardware-rev5p0).
4. ModPrsL can be implemented as a short-circuit to the GND on the module.

Optical Characteristics

Parameter		Min.	Typ.	Max.	Unit	Notes
Transmitter						
Modulation Format	**400G**	ZR400-CFEC-16QAM				CFEC FEC, NCG 10.8dB
		ZR400-OFEC-16QAM				OFEC FEC, NCG 11.6dB
Baud Rate	**400G**	59.843750000 ± 20ppm			GBd	400ZR, SFF-8024 Media ID 3Fh
		60.138546798 ± 20ppm			GBd	400ZR+, SFF-8024 Media ID 46h
Transmitter Frequency Range			193.7		THz	1
Laser Frequency Accuracy		-1.8		1.8	GHz	
Tx Spectral Upper Mask				(30.0, 0.0) (37.0,-1 0.0) (39.2,-1 5.0) (40.4,-2 0.0)	(GHz,dB)	2
Tx Spectral Lower Mask		(30.0,-9.0) (31.3,-2 0.0) (31.3,-3 5.0)			(GHz,dB)	3
Transmitter Laser Disable Time				100	ms	
Transmitter Laser Enable Time				10	s	
Transmit Output Power		-9		-6	dBm	For OIF 400ZR app code 0x02
Output Power Monitor Accuracy		-1		1	dB	
Power Stability		-0.5		0.5	dB	At fixed wavelength, room temperature
		-1		1	dB	At fixed wavelength
Total Output Power with Tx Disabled				-20	dBm	
Total Output Power During Wavelength Switching				-20	dBm	
Transmitter Reflectance				-20	dB	Looking into the Tx
In-Band (IB) OSNR		40			dB	
Out-of-Band (OOB) OSNR		35			dB	
Lorentzian Linewidth				300	kHz	Tx and LO
Relative Intensity Noise				-140	dB/Hz	
Mean I-Q Amplitude Imbalance				1	dB	
Transmitter Polarization-Dependent Power				1.5	dB	
DC I-Q Offset (Mean Per Polarization)				-26	dB	
I-Q Instantaneous Offset				-20	dB	
Receiver						
Modulation Format	**400G**	ZR400-CFEC-16QAM				4
		ZR400-OFEC-16QAM				5

Baud Rate	**400G**	59.843750000 ± 20ppm			GBd	400ZR, SFF-8024 Media ID 3Fh	
		60.138546798 ± 20ppm			GBd	400ZR+, SFF-8024 Media ID 46h	
Frequency Offset Between Received Carrier and LO		-3.6		3.6	GHz		
Rx Sensitivity	**400G**	-21			dBm	400ZR	6
		-23			dBm	400ZR+	7
Non-Damaging Input Power				10	dBm	Total power	
Optical Input Power Monitor Accuracy		-2		2	dB	Total power	
Maximum Pre-FEC BER		0.017		0.020			
Chromatic Dispersion Tolerance	**400G**			2400	ps/nm	400ZR	Tolerance to CD with ≤0.5dB Rx sensitivity
				2400	ps/nm	400ZR+	
CD Monitor Accuracy		-200		200	ps/nm		
DGD Tolerance	**400G**	33			ps	400ZR	Rx Sensitivity penalty <0.5dB when change in SOP is ≤ 1rad/ms
		33			ps	400ZR+	
DGD Monitor Accuracy		-15		15	ps	0 to 40ps for 400ZR 0 to 100ps for 400/300/200/100ZR+	
Peak PDL Tolerance				1.5	dB	8	
Tolerance to Change in SOP		50			krad/s	9	
Optical Return Loss		20			dB	10	
Optical Rx_LOS Assert Threshold	**400G**	-28	-26	-24	dBm	OIF 400ZR	
		-30	-28	-36	dBm	400ZR+	
Optical Rx_LOS Hysteresis		1	1.5	2.5	dB		
Service Recovery Time				40	ms		

Notes:

1. For OIF 400ZR app code 0x02, the frequency is fixed at 193.7THz and not configurable.
2. Refer to OIF-400ZR-02.0 13.3.201a. Refer to openzrplus_2p0 11.4.10.
3. Refer to OIF-400ZR-02.0 13.3.201b. Refer to openzrplus_2p0 11.4.10.
4. CFEC FEC, Net Coding Gain (NCG) 10.8dB, Theoretical Max. Pre-FEC BER $1.25E^{-2}$.
5. OFEC FEC, Net Coding Gain (NCG) 11.6dB, Theoretical Max. Pre-FEC BER $2.0E^{-2}$.
6. In-Band (IB) OSNR ≥ 34dB, OIF 400ZR app code 0x02.
7. In-Band (IB) OSNR ≥ 34dB.
8. Tolerance to change in peak PDL with < 0.4dB Rx sensitivity penalty when change in SOP is ≤1rad/ms.
9. Tolerance to change in SOP with <0.3dB additional power penalty over all PMD and PDL.
10. Optical reflectance at Rx connector input.

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInitDuration	MaxMgmtInit		2000	ms	1
ResetL Assert Time	t_reset_init	10		us	2
IntL Assert Time	ton_IntL		200	ms	3
IntL De-Assert Time	toff_IntL		500	us	4
Rx LOS Assert Time	ton_los		100	ms	5
Rx LOS Assert Time (Optional Fast-Mode)	ton_losf		10	ms	6
Rx LOS De-Assert Time	toff_los		100	ms	
Tx Fault Assert Time	ton_Txfault		200	ms	7
Flag Assert Time	ton_flag		200	ms	8
Mask Assert Time	ton_mask		100	ms	9
Mask De-Assert Time	toff_mask		100	ms	10
High Power Up State			180	s	
Software Tx Disable Assert Time			100	ms	
Software Tx Disable De-Assert Time			10	s	

Notes:

1. Time from power on, hot-plug, or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until VOUT:IntL=VOL.
4. Time from clear on read operation of associated flag until VOUT:IntL=VOH. This includes de-assert times for Rx_LOS, Tx_Fault, and other flag bits.
5. Time from Rx_LOS condition present to Rx_LOS bit set (value = 1b) and IntL asserted.
6. Time from Rx_LOS state to Rx_LOS bit set (value = 1b) and IntL asserted.
7. Time from Tx_Fault state to Tx_Fault bit set (value=1b) and IntL asserted.
8. Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
9. Time from mask bit set (value=1b) until associated IntL assertion is inhibited.
10. Time from mask bit cleared (value=0b) until associated IntL operation resumes.

Pin Descriptions

Pin	Symbol	Logic	Name/Description	Plug Sequence	Notes
1	GND		Module Ground.	1B	1
2	Tx2-	CML-I	Transmitter Inverted Data Input.	3B	
3	Tx2+	CML-I	Transmitter Non-Inverted Data Input.	3B	
4	GND		Module Ground.	1B	1
5	Tx4-	CML-I	Transmitter Inverted Data Input.	3B	
6	Tx4+	CML-I	Transmitter Non-Inverted Data Input.	3B	
7	GND		Module Ground.	1B	1
8	ModSelL	LVTTL-I	Module Select.	3B	
9	ResetL	LVTTL-I	Module Reset.	3B	
10	VccRx		+3.3V Receiver Power Supply.	2B	2
11	SCL	LVCMOS-I/O	2-Wire Serial Interface Clock.	3B	
12	SDA	LVCMOS-I/O	2-Wire Serial Interface Data.	3B	
13	GND		Module Ground.	1B	1
14	Rx3+	CML-O	Receiver Non-Inverted Data Output.	3B	
15	Rx3-	CML-O	Receiver Inverted Data Output.	3B	
16	GND		Module Ground.	1B	1
17	Rx1+	CML-O	Receiver Non-Inverted Data Output.	3B	
18	Rx1-	CML-O	Receiver Inverted Data Output.	3B	
19	GND		Module Ground.	1B	1
20	GND		Module Ground.	1B	1
21	Rx2-	CML-O	Receiver Inverted Data Output.	3B	
22	Rx2+	CML-O	Receiver Non-Inverted Data Output.	3B	
23	GND		Module Ground.	1B	1
24	Rx4-	CML-O	Receiver Inverted Data Output.	3B	
25	Rx4+	CML-O	Receiver Non-Inverted Data Output.	3B	
26	GND		Module Ground.	1B	1
27	ModPrsL	LVTTL-O	Module Present.	3B	
28	IntL	LVTTL-O	Interrupt.	3B	
29	VccTx		+3.3V Transmitter Power Supply.	2B	2
30	Vcc1		+3.3V Power Supply.	2B	2
31	LPMODE	LVTTL-I	Low-Power Mode.	3B	
32	GND		Module Ground.	1B	1
33	Tx3+	CML-I	Transmitter Non-Inverted Data Input.	3B	
34	Tx3-	CML-I	Transmitter Inverted Data Input.	3B	
35	GND		Module Ground.	1B	1
36	Tx1+	CML-I	Transmitter Non-Inverted Data Input.	3B	
37	Tx1-	CML-I	Transmitter Inverted Data Input.	3B	
38	GND		Module Ground.	1B	1
39	GND		Module Ground.	1A	1
40	Tx6-	CML-I	Transmitter Inverted Data Input.	3A	
41	Tx6+	CML-I	Transmitter Non-Inverted Data Input.	3A	

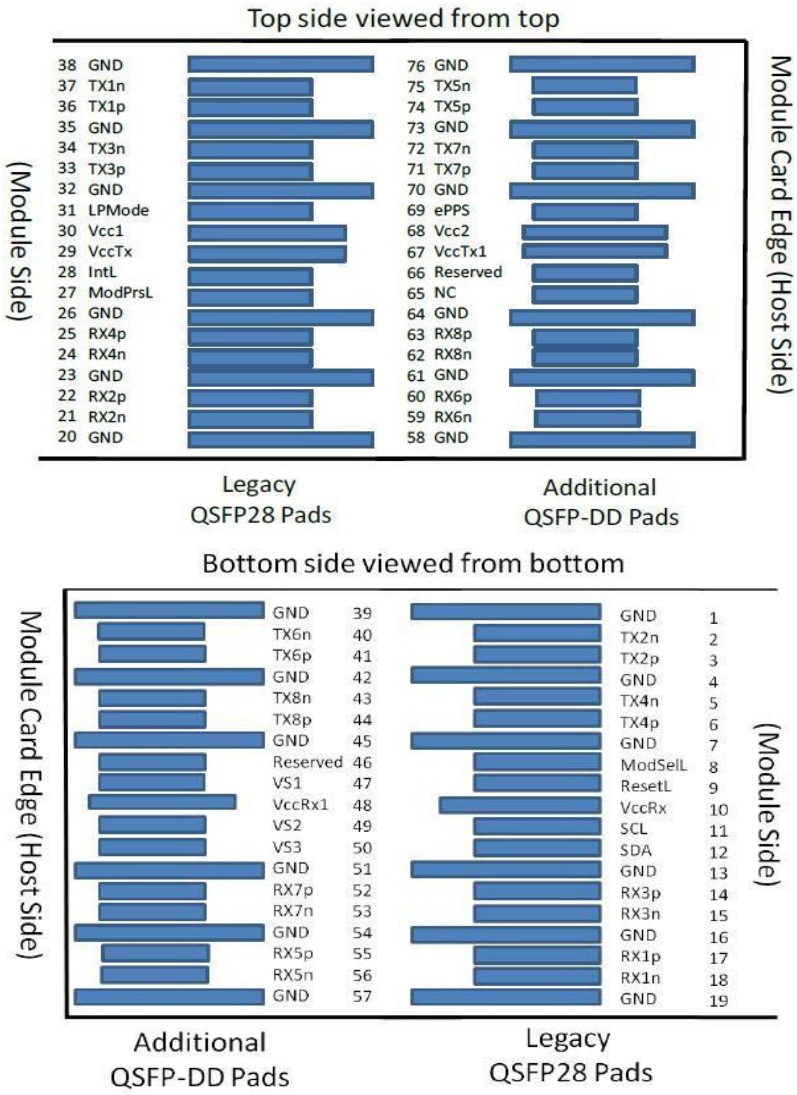
42	GND		Module Ground.	1A	1
43	Tx8-	CML-I	Transmitter Inverted Data Input.	3A	
44	Tx8+	CML-I	Transmitter Non-Inverted Data Input.	3A	
45	GND		Module Ground.	1A	1
46	Reserved		For Future Use.	3A	3
47	VS1		Module Vendor-Specific 1.	3A	3
48	VccRx1		+3.3V Receiver Power Supply.	2A	2
49	VS2		Module Vendor-Specific 2.	3A	3
50	VS3		Module Vendor-Specific 3.	3A	3
51	GND		Module Ground.	1A	1
52	Rx7+	CML-O	Receiver Non-Inverted Data Output.	3A	
53	Rx7-	CML-O	Receiver Inverted Data Output.	3A	
54	GND		Module Ground.	1A	1
55	Rx1+	CML-O	Receiver Non-Inverted Data Output.	3A	
56	Rx1-	CML-O	Receiver Inverted Data Output.	3A	
57	GND		Module Ground.	1A	1
58	GND		Module Ground.	1A	1
59	Rx6-	CML-O	Receiver Inverted Data Output.	3A	
60	Rx6+	CML-O	Receiver Non-Inverted Data Output.	3A	
61	GND		Module Ground.	1A	1
62	Rx8-	CML-O	Receiver Inverted Data Output.	3A	
63	Rx8+	CML-O	Receiver Non-Inverted Data Output.	3A	
64	GND		Module Ground.	1A	1
65	NC		Not Connected.	3A	3
66	Reserved		For Future Use.	3A	3
67	VccTx1		+3.3V Transmitter Power Supply.	2A	2
68	Vcc2		+3.3V Power Supply.	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) Reference Clock Input. Not Used.	3A	3
70	GND		Module Ground.	1A	1
71	Tx7+	CML-I	Transmitter Non-Inverted Data Input.	3A	
72	Tx7-	CML-I	Transmitter Inverted Data Input.	3A	
73	GND		Module Ground.	1A	1
74	Tx5+	CML-I	Transmitter Non-Inverted Data Input.	3A	
75	Tx5-	CML-I	Transmitter Inverted Data Input.	3A	
76	GND		Module Ground.	1A	1

Notes:

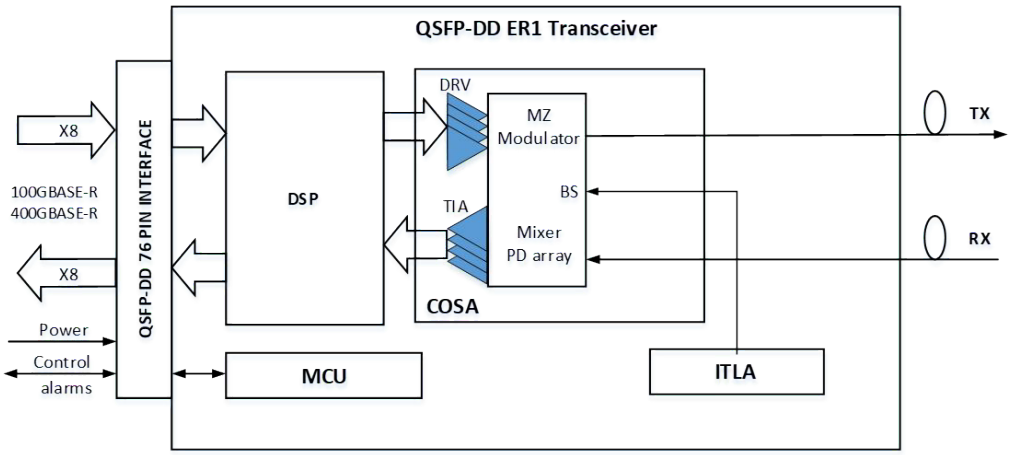
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500mA.

3. All Vendor-Specific, Reserved, and Not Connected pins may be terminated with 50Ω to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact Sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

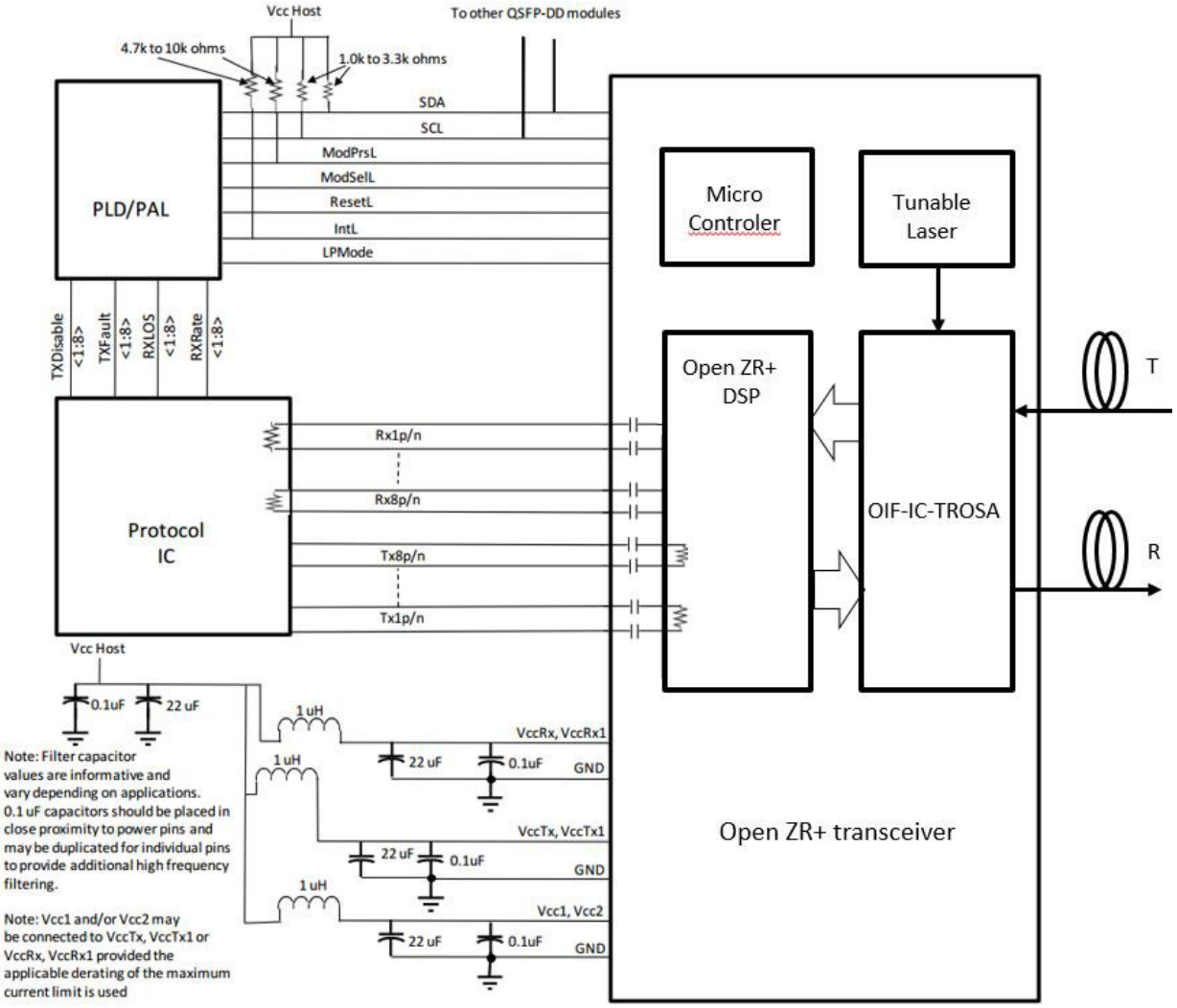
Electrical Pad Layout



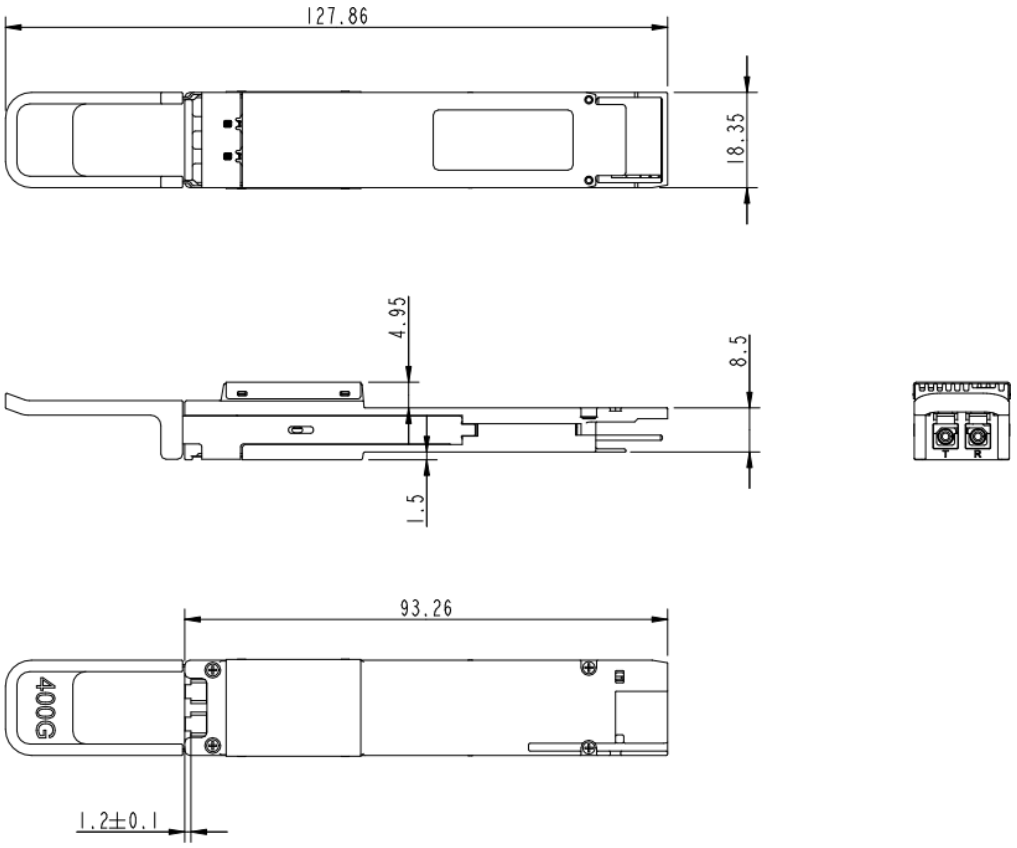
Block Diagram



Recommended Interface Circuit



Mechanical Specifications



About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.