



QBPOD010E00FB7F

Cisco® QDD-400G-LR8-S Compatible 400GBase-LR8 PAM4 QSFP-DD Transceiver (SMF, 1270nm to 1330nm, 10km, LC, DOM, CMIS 4.0)

Product Description

This Cisco® QDD-400G-LR8-S compatible QSFP-DD transceiver provides 400GBase-LR8 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1270nm to 1330nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Cisco® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

Features:

- Hot-pluggable QSFP-DD Type 2 form factor
- Power dissipation < 13W
- Supports 425Gb/s aggregate bit rate
- Single-mode Fiber
- Aligned with IEEE 802.3bs
- Single 3.3V power supply
- Operating case temperature: 0C to 70C



Applications:

- 400GBase Ethernet
- Access and Enterprise

For your product safety, please read the following information carefully before any manipulation of the transceiver:



ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Power Supply Voltage	VCC	-0.5	4.0	V	
Storage Temperature	Ts	-40	+85	°C	
Case Operating Temperature	Top	0	+70	°C	
Relative Humidity (non-condensing)	RH	15	85	%	
Receiver Damage Threshold, per Lane	P _{Rdmg}	6.3		dBm	
Bit Rate (all wavelengths combined)	BR		425	Gb/s	1
Bit Error Ratio	BER		2.4x10 ⁻⁴		2
Maximum Supported Distances					
Fiber Type					
SMF per G.652	L _{max1}		10	km	

Notes:

1. Supports 400GBASE-LR8 per IEEE P802.3bs.
2. As defined by IEEE P802.3bs.

Electrical Characteristics (EOL, T_{OP} = 0 to +70°C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Supply Current	I _{CC}			3.83	A	
Module total power	P			13	W	1
Transmitter						
Signaling Rate, each Lane	V _{in} , pp, diff	26.5625 ± 100 ppm			GBd	
Differential data input voltage per lane	TP1a	900			mVpp	1
Differential input return loss		Per equation (83E-5) IEEE802.3bm			dB	
Differential to common mode input return loss		Per equation (83E-6) IEEE802.3bm			dB	
Differential termination mismatch				10	%	
Module stress input test		Per 120E.3.4.1 IEEE802.3bs				3
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	4
Receiver						
Signaling Rate, each lane		26.5625 ± 100 ppm			GBd	
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	dB	
Differential output return loss		Per equation 83E-2 IEEE802.3bm				
Common to differential mode conversion return loss		Per equation 83E-3 IEEE802.3bm				
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage (min)		-350		2850	mV	4

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets specified BER
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics (EOL, T_{OP} = 0 to +70°C, V_{CC} = 3.135 to 3.465 Volts)

Meets 400GBASE-LR8 as being defined by IEEE P802.3bs

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling rate (each lane (range))		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Lane wavelengths (range)		1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19			nm	
Side-mode suppression ratio (SMSR)		30			dB	
Total average launch power				13.2	dBm	
Average launch power, each lane				5.3	dBm	1
Average launch power, each lane		-2.8			dBm	2
Outer Optical Modulation Amplitude (OMA _{outer}), each lane		0.2		5.7	dBm	3
Difference in launch power between any two lanes (OMA _{outer})				4	dB	
Launch power in OMA _{outer} minus TDECQ, each lane		-1.1			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.3	dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction ratio		3.5			dB	
RIN _{15,1} OMA				-132	dB/Hz	
Optical return loss tolerance				15.1	dB	
Transmitter reflectance				-26	dB	4
Receiver						
Signaling rate (each lane (range))		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Lane wavelengths (range)		1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19			nm	
Damage threshold, each lane		6.3			dBm	5
Average receive power, each lane				5.3	dBm	
Average receive power, each lane		-9.1			dBm	6
Receive power (OMA _{outer}), each lane				5.7	dBm	

Difference in receive power between any two lanes (OMAouter)				4.5	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane				-7.1	dBm	7
Stressed receiver sensitivity (OMAouter), each lane				-4.7	dBm	8
Conditions for Stress Receiver Sensitivity Test						
Stressed eye closure for PAM4 (SECQ), lane under test		3.3			dB	9
OMAouter of each aggressor lane		-0.2			dBm	9

Notes:

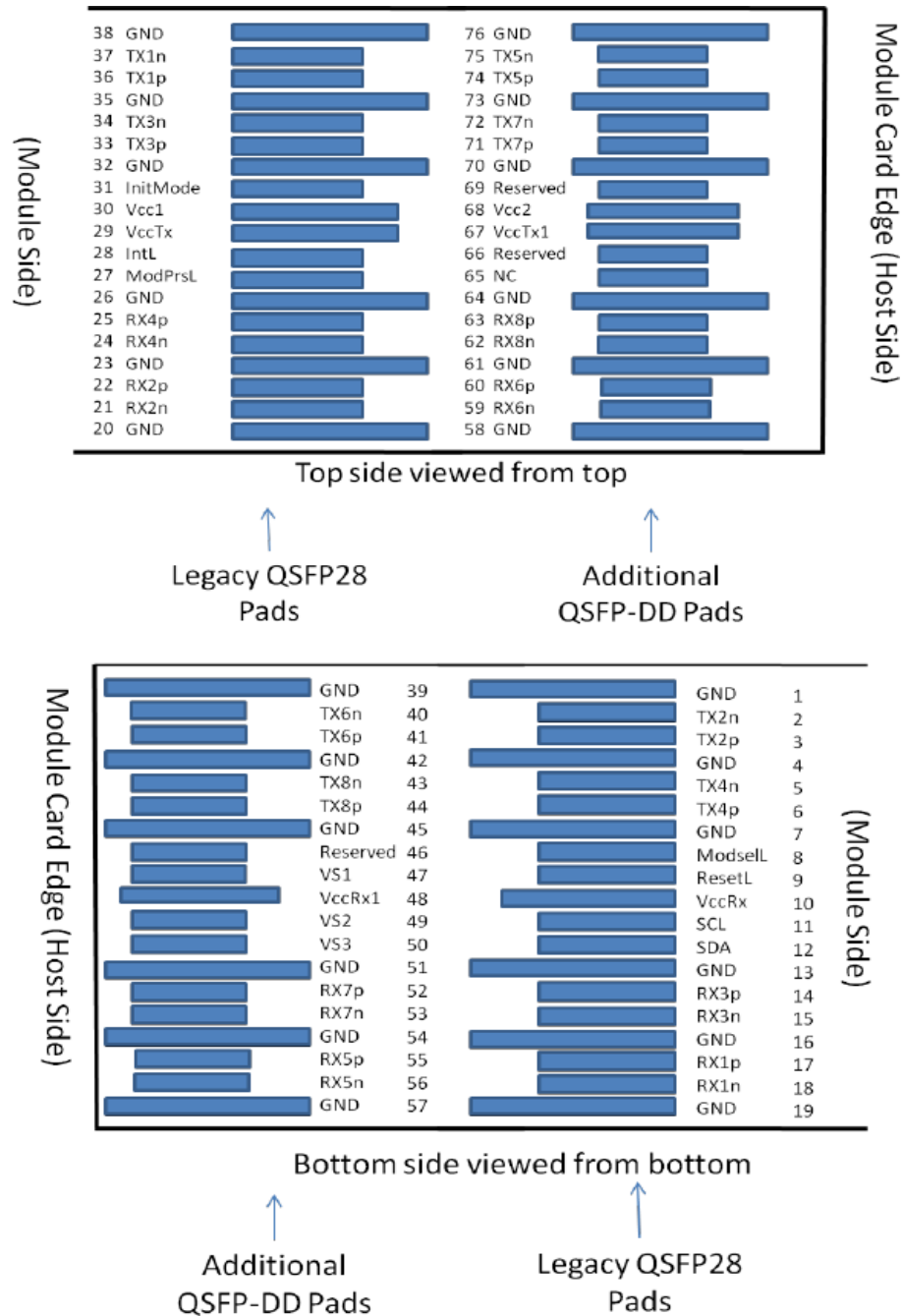
1. As the total average launch power limit has to be met, not all of the lanes can operate at the maximum average launch power, each lane.
2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Even if the TDECQ < 1 dB, the OMAouter (min) must exceed this value
4. Transmitter reflectance is defined looking into the transmitter
5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Receiver sensitivity (OMAouter), each lane (max) is informative.
8. Measured with conformance test signal at TP3 (see 122.8.9) for the BER specified in 122.1.1.
9. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Descriptions

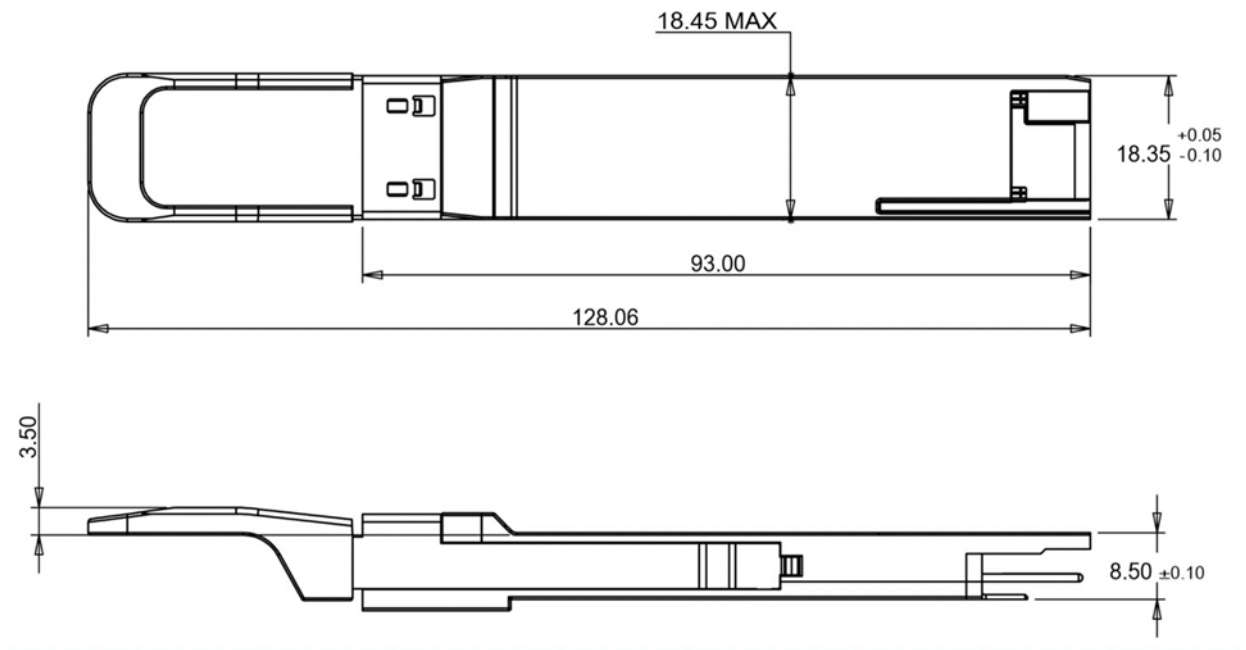
Pin	Logic	Symbol	Name/Descriptions	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
67		GND	Ground	1A
68		NC	No Connect	3A
69		Reserved	For future use	3A
70		VccTx1	3.3V Power Supply	2A
71		Vcc2	3.3V Power Supply	2A
72		Reserved	For Future Use	3A
73		GND	Ground	1A
74	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx7n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

MSA Compliant Connector



Mechanical Specifications



About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.

