



## Q28C-100G-DCO-0DB-I-SKY

MSA Compliant (with select systems) 100GBase-ZR QSFP28 Transceiver (SMF, 1528.77nm to 1567.13nm, 80km, LC, DOM, -40 to 85C, 0dbm, CMIS)

### Product Description

This MSA compliant (with select systems) high Tx power 0dBm QSFP28 transceiver provides 100GBase-ZR throughput up to 80km over single-mode fiber (SMF) using a wavelength of 1528.77nm to 1567.13nm via an LC connector. It can operate at temperatures between -40 and 85C. Our transceiver is built to meet or exceed OEM specifications. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

### Features:

- Hot-Pluggable QSFP28 Form Factor
- IEEE 100G Ethernet (CAUI-4) or ITU-T 100G OTN (OTL4.4) Compliant Host Interface
- CMIS 5.2
- Full C-Band Tunable, 50GHz/100GHz Spacing
- Operating Temperature: -40 to 85 Celsius
- Transmission Reach up to 80km Unamplified (Loss Limited) or up to 120km Amplified (Dispersion Limited, Optionally Extendable to 300km)
- RoHS Compliant and Lead-Free
- Power Dissipation: 6.7W
- Please contact your sales representative for specific system information



### Applications:

- 100GBase Ethernet
- Duplex Mux

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*For your product safety, please read the following information carefully before any manipulation of the transceiver:*



#### ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



#### LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

*The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.*

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## Absolute Maximum Ratings

| Parameter                                      |           | Symbol             | Min. | Typ. | Max. | Unit | Notes |
|------------------------------------------------|-----------|--------------------|------|------|------|------|-------|
| DC Supply Voltage                              |           | V <sub>cc</sub>    | -0.3 |      | 3.6  | V    |       |
| Low-Speed I/O Voltages                         |           |                    | -0.3 |      | 3.6  | V    |       |
| Storage Temperature                            |           | T <sub>stg</sub>   | -40  |      | 85   | °C   |       |
| Operating Case Temperature                     | Long-Term | T <sub>c</sub>     | -20  |      | 85   | °C   |       |
|                                                | Start-Up  |                    | -40  |      | 85   | °C   |       |
| Operating Relative Humidity                    |           | RH                 | 5    |      | 95   | %    |       |
| Rx Input Power                                 |           | PR <sub>x,in</sub> |      |      | 10   | dBm  |       |
| ESD Damage Threshold<br>Human Body Model (HBM) | DC Pins   |                    | 2000 |      |      | V    |       |
|                                                | RF Pins   |                    | 1000 |      |      | V    |       |

## Notes:

- Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the datasheet. Exposure to Absolute Maximum Ratings for extended periods of time can adversely affect device reliability. Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Host Interface Modes

| Host Interface ID [18] | Host Interface Description [18]     | Modulation | Forward Error Correction Code | Nominal Symbol Rate (GBd) | Supported Line Interface IDs [18] |
|------------------------|-------------------------------------|------------|-------------------------------|---------------------------|-----------------------------------|
| 65 [9]                 | CAUI-4 C2M without FEC              | NRZ        | None                          | 25.78125                  | 68, 192, 193                      |
| 66 [9]                 | CAUI-4 C2M with RS(528,514) FEC     | NRZ        | RS(528,514)                   | 25.78125                  | 68, 192, 193                      |
| 57 [10]                | OTL4.4 (ITU-T G.709/ Y1331 G.Sup58) | NRZ        | RS(255, 239)                  | 27.9525                   | 192, 193                          |

## Electrical Characteristics

| Parameter                     | Symbol              | Min.  | Typ. | Max.  | Unit | Notes                                           |
|-------------------------------|---------------------|-------|------|-------|------|-------------------------------------------------|
| Power Supply – General        |                     |       |      |       |      |                                                 |
| Power Supply Voltages         |                     | 3.135 | 3.3  | 3.465 | V    | Including ripple, droop, and noise below 100kHz |
| Host RMS Noise Output         |                     |       |      | 25    | mV   | 10Hz - 10MHz                                    |
| Module RMS Noise Output       |                     |       |      | 15    | mV   | 10Hz - 10MHz                                    |
| Module Supply Noise Tolerance | PSNR <sub>mod</sub> |       |      | 66    | mV   | 10Hz - 10MHz, peak-to-peak                      |
| Module In-Rush                | Tip                 |       |      | 50    | μs   | Instantaneous peak duration                     |
|                               | T <sub>init</sub>   |       |      | 500   | ms   | Initialization time                             |
| Power Supply – Low-Power Mode |                     |       |      |       |      |                                                 |
| Power Dissipation             | Plp                 |       |      | 1.5   | W    |                                                 |

|                                                          |                   |           |         |      |         |     |                                                |
|----------------------------------------------------------|-------------------|-----------|---------|------|---------|-----|------------------------------------------------|
| Power Supply Current                                     |                   | Icc,ip,lp |         |      | 600     | mA  | Instantaneous peak current                     |
|                                                          |                   | Icc,sp,lp |         |      | 495     | mA  | Sustained peak current                         |
|                                                          |                   | Icc,lp    |         |      | 478     | mA  | 1, steady state current                        |
| Power Supply – High-Power Mode – 2.4ns/nm CD             |                   |           |         |      |         |     |                                                |
| Power Dissipation                                        |                   | Php       |         | 6.0  | 6.7     | W   |                                                |
| Power Supply Current                                     |                   | Icc,ip,hp |         |      | 2600    | mA  | Instantaneous peak current                     |
|                                                          |                   | Icc,sp,hp |         |      | 2212    | mA  | Sustained peak current                         |
|                                                          |                   | Icc,hp    |         |      | 2137    | mA  | 1, steady state current                        |
| Power Supply – High-Power Mode – 6.0ns/nm CD             |                   |           |         |      |         |     |                                                |
| Power Dissipation                                        |                   | Php       |         | 6.3  | 6.9     | W   |                                                |
| Power Supply Current                                     |                   | Icc,ip,hp |         |      | 2600    | mA  | Instantaneous peak current                     |
|                                                          |                   | Icc,sp,hp |         |      | 2308    | mA  | Sustained peak current                         |
|                                                          |                   | Icc,hp    |         |      | 22233   | mA  | 1, steady state current                        |
| Low-Speed I/O                                            |                   |           |         |      |         |     |                                                |
| Clock Frequency (SCL)                                    |                   | fSCL      |         | 400  |         | kHz | Default                                        |
|                                                          |                   |           |         | 1000 |         |     | Fast-mode+                                     |
| Output Voltage (SCL and SDA)                             |                   | VOL       | 0.0     |      | 0.4     |     | Output low                                     |
|                                                          |                   | VOH       | Vcc-0.5 |      | Vcc+0.3 |     | Output high                                    |
| Input Voltage (SCL and SDA)                              |                   | VIL       | -0.3    |      | 0.63    | V   | Input low                                      |
|                                                          |                   | VIH       | 0.7×Vcc |      | Vcc+0.5 |     | Input high                                     |
| Capacitance for SCL and SDA I/O Signal                   |                   | Ci        |         |      | 14      | pF  |                                                |
| Total Bus Capacitive Load for SCL and SDA                | 400kHz Clock Rate | Cb        |         |      | 100     | pF  | 2, 3.0kΩ pull-up resistor, maximum             |
|                                                          |                   |           |         |      | 200     |     | 2, 1.6kΩ pull-up resistor, maximum             |
| Input Voltage/Current, LPMode/TxDis, ResetL, and ModSelL |                   | VIL       | -0.3    |      | 0.8     | V   | Input voltage, low                             |
|                                                          |                   | VIH       | 2.0     |      | Vcc+0.3 |     | Input voltage, high                            |
|                                                          |                   | Iin       | -365    |      | 125     | μA  | Input current, 0V < VIN < Vcc                  |
| Output Voltage, ModPrsL, and IntL/RxLOSL                 |                   | VOL       | 0.0     |      | 0.4     | V   | Output low, IOL = 2mA                          |
|                                                          |                   | VOH       | Vcc-0.5 |      | Vcc+0.3 |     | Output high, 10kΩ pull-up resistor to Host Vcc |

**Notes:**

1. The module will stay within its advertised power class for all supply voltages.
2. For 1000kHz clock rate.

## Optical Characteristics

| Parameter                                               | Symbol           | Min.     | Typ.  | Max.  | Unit       | Notes                                                                 |
|---------------------------------------------------------|------------------|----------|-------|-------|------------|-----------------------------------------------------------------------|
| Power Supply – General                                  |                  |          |       |       |            |                                                                       |
| Symbol Rate                                             | Rbaud            |          | 27.95 |       | GBd        |                                                                       |
| Modulation Format                                       |                  | DP-DQPSK |       |       |            |                                                                       |
| Channel Frequency Range                                 | Vc               | 191.4    | 193.7 | 196.1 | THz        | 100GHz grid                                                           |
|                                                         | Vc               | 191.35   | 193.7 | 196.1 | THz        | 50GHz grid                                                            |
| Channel Spacing                                         | $\Delta Vc$      |          | 100   |       | GHz        | 100GHz grid                                                           |
|                                                         | $\Delta Vc$      |          | 50    |       | GHz        | 50GHz grid                                                            |
| Frequency Accuracy                                      | $\delta Vc$      | -1.8     |       | 1.8   | GHz        |                                                                       |
| Laser Intrinsic Linewidth                               | LW               |          |       | 500   | kHz        | Calculated based on FM noise Power Spectral Density (PSD) measurement |
| Side-Mode Suppression Ratio                             | SMSR             | 40       |       |       | dB         | No modulation                                                         |
| Relative Intensity Noise                                | RIN              |          |       | -140  | dB/Hz      | Peak over 0.2GHz < f < 10GHz                                          |
| Transmitter                                             |                  |          |       |       |            |                                                                       |
| Tx Output Power                                         | PTx,out          | 0        |       | 3     | dBm        |                                                                       |
| Tx Output Power Monitor Range                           | PTx,mon          | -2       |       | 4     | dBm        |                                                                       |
| Tx Output Power Monitor Accuracy                        | $\delta PTx,mon$ | -1.5     |       | 1.5   | dB         | Tx optical power monitor reading relative to actual Tx output power   |
| Tx Output Power During Tuning or when Tx is Disabled    | PTx,dark         |          |       | -35   | dBm        |                                                                       |
| Tx Spectral Excursion                                   |                  | -15      |       | 15    | GHz        | ITU-T G.698.2 §7.2.3 [11]                                             |
| Tx Output Power Imbalance Between X and Y Polarizations | $\Delta PX/Y$    |          |       | 1.5   | dB         |                                                                       |
| Tx XY Skew                                              |                  |          |       | 6.0   | ps         |                                                                       |
| Tx IQ Offset                                            |                  |          |       | -25   | dB         |                                                                       |
| Tx IQ Imbalance                                         |                  |          |       | 1.0   | dB         |                                                                       |
| Tx Quadrature Error                                     |                  | -7.0     |       | 7.0   | °          |                                                                       |
| Tx IQ Skew                                              |                  |          |       | 1.5   | ps         |                                                                       |
| Tx Error Vector Magnitude Mask Ratio                    |                  |          |       | 23    | %          | ITU-T G.698.2 §7.2.12 [11], with 24dB/12.5GHz noise loading           |
| Tx In-Band Optical Signal to Noise Ratio                | OSNRin           | 39       |       |       | dB/12.5GHz | Under modulation, $ \Delta f  < 60\text{GHz}$                         |
| Tx Out-of-Band Optical Signal to Noise Ratio            | OSNRout          | 30       |       |       | dB/12.5GHz | Under modulation, $ \Delta f  > 150\text{GHz}$                        |
| Tx Reflectance                                          |                  |          |       | -20   | dB         |                                                                       |
| Receiver                                                |                  |          |       |       |            |                                                                       |
| Rx Total Input Power                                    | PRx,tot          | -30      |       | 3     | dBm        | Broadband                                                             |
| Rx Signal Input Power (Amplified)                       | PRx,sig          | -18      |       | 1     | dBm        | Full Rx OSNR tolerance                                                |
|                                                         |                  | -22      |       | 3     | dBm        | 1                                                                     |

|                                                   |               |             |      |  |     |            |                                                     |
|---------------------------------------------------|---------------|-------------|------|--|-----|------------|-----------------------------------------------------|
| Rx OSNR Tolerance                                 | 100G DQPSK SC |             | 16.5 |  |     | dB/12.5GHz | 2                                                   |
| CD Tolerance                                      |               |             |      |  | 2.4 | ns/nm      | Default, OSNR penalty < 0.5dB                       |
|                                                   |               |             |      |  | 6.0 |            | 3                                                   |
| PMD Tolerance                                     |               |             |      |  | 10  | Ps         | 4                                                   |
| DGD Tolerance                                     |               |             |      |  | 30  | Ps         | 4                                                   |
| Tolerance to Change in SOP                        |               |             |      |  | 50  | krad/s     | 4                                                   |
| PDL OSNR Penalty                                  | 1dB PDL       |             |      |  | 0.5 | dB/12.5GHz | Change in principal state of polarization < 1rad/ms |
|                                                   | 2dB PDL       |             |      |  | 1.0 |            |                                                     |
|                                                   | 4dB PDL       |             |      |  | 3.0 |            |                                                     |
| Rx Signal Input Power Transient Amplitude         |               |             | -3   |  | 3   | dB         | 5                                                   |
| Rx Signal Input Power Transient Rise/Fall Time    |               |             | 100  |  |     | μs         | 6                                                   |
| Colorless Drop OSNR Penalty                       |               |             |      |  | 0.5 | dB         | 7                                                   |
| Colorless Drop Adjacent Channel Crosstalk Penalty |               |             |      |  | 0.2 | dB         | 8                                                   |
| Rx Signal Input Power (Unamplified)               | 100G DQPSK SC |             | -30  |  | 1   | dBm        | OSNR > 35dB/12.5GHz                                 |
| Rx Signal Input Power Monitor Range               |               | PRx,mon(s)  | -21  |  | 3   | dBm        |                                                     |
| Rx Signal Input Power Monitor Accuracy            |               | δPRx,mon(s) | -2.5 |  | 2.5 | dB         |                                                     |
| Rx Total Input Power Monitor Range                |               | PRx,mon(t)  | -21  |  | 6   | dBm        |                                                     |
| Rx Total Input Power Monitor Accuracy             |               | δPRx,mon(t) | -2.0 |  | 2.0 | dB         |                                                     |
| Rx Reflectance                                    |               |             |      |  | -20 | dB         |                                                     |
| Rx Synch Time                                     |               |             |      |  | 30  | ms         |                                                     |

#### Notes:

1. Extended range. Rx signal input power range over which performance can be guaranteed with <1dB OSNR penalty relative to the Rx OSNR tolerance limit.
2. Back-to-back, PRx,sig > -18dBm. Rx OSNR tolerance for Carrier Frequency Offset |CFO| <1GHz. Up to 1dB penalty for worst case |CFO| = 3.6GHz.
3. Extended, OSNR penalty <1.0dB. Power dissipation will increase by approximately 0.2W if extended CD compensation is enabled.
4. OSNR penalty <0.5dB.
5. Peak excursion from steady state, transient within Rx signal input power (amplified) range and OSNR penalty <0.5dB.
6. Rise/fall time for the above peak excursion, OSNR penalty <0.5dB.
7. Rx total input power to signal input power ratio <12dB. Receiver is able to tolerate the specified ratio of total power of crosstalk channels and ASE to signal power with the specified OSNR penalty. Does not include contribution from adjacent channel crosstalk. No single channel power exceeding signal channel power by more than 1dB shall be included. Measured at Rx signal input power -6dBm.
8. Measured at the Rx OSNR limit, 50GHz channel spacing, both adjacent channels <1dB higher power than signal channel.

## Common Management Interface Specifications (CMIS)

| Parameter                          | Symbol                     | Min. | Max. | Unit | Conditions                                                                                                                                                     | Notes |
|------------------------------------|----------------------------|------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| MgmtInitDuration                   |                            |      | 2000 | ms   | Time from power on, hot plug , or rising edge of reset until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction. | 1     |
| ResetL Assert Time                 |                            | 10   |      | μs   | Minimum pulse time on the ResetL signal to initiate a module reset.                                                                                            |       |
| IntL/RxLOS Mode Change Time        |                            |      | 100  | ms   | Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL.                                                                              |       |
| LPMODE/TxDis Mode Change Time      |                            |      | 100  | ms   | Time to change between LPMODE and TxDis modes of the LPMODE/TxDis signal.                                                                                      |       |
| IntL Assert Time                   |                            |      | 200  | ms   | Time from occurrence of condition triggering IntL until Vout:intL=Vol                                                                                          |       |
| IntL De-Assert Time                |                            |      | 500  | μs   | Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes de-assert times for Rx LOS, Tx Fault, and other flag bits.             | 2     |
| RxLOS Assert Time                  |                            |      | 1    | ms   | Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.                                                                           | 3     |
| RxLOS De-Assert Time               |                            |      | 3    | ms   | Time from optical signal above the LOS de-assert threshold to when the module releases the RxLOS signal to high.                                               |       |
| Tx Disable Assert Time             |                            |      | 1    | ms   | Time from Tx Disable bit set (value = 1b) until optical output falls below 10% of nominal.                                                                     | 4     |
| Tx Disable De-Assert Time          |                            |      | 10   | s    | Time from Tx Disable bit cleared (value = 0b) until optical output rises above 90% of nominal.                                                                 | 4     |
| Tx Fault Assert Time               |                            |      | 200  | ms   | Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted.                                                                                   |       |
| Flag Assert Time                   |                            |      | 200  | ms   | Time from occurrence and condition triggering flag to associated flag bit set (value = 1b) and IntL asserted.                                                  |       |
| Mask Assert Time                   |                            |      | 100  | ms   | Time from mask bit set (value = 1b) until the associated IntL assertion is inhibited.                                                                          | 5     |
| Mask De-Assert Time                |                            |      | 100  | ms   | Time from mask bit cleared (value = 0b) until associated IntL operation resumes.                                                                               | 5     |
| Data Path Tx Turn On Max Duration  | See CMIS memory P01h: B168 |      |      |      | Maximum duration of Tx Turn On state.                                                                                                                          | 6     |
| Data Path Tx Turn Off Max Duration | See CMIS memory P01h: B168 |      |      |      | Maximum duration of Tx Turn Off state.                                                                                                                         | 6     |
| Data Path Deinit Max Duration      | See CMIS memory P01h: B144 |      |      |      | Maximum duration of DataPathDeInit state.                                                                                                                      | 6     |
| Data Path Init Max Duration        | See CMIS memory P01h: B144 |      |      |      | Maximum duration of DataPathInit state.                                                                                                                        | 6     |
| Module Pwr Up Max Duration         | See CMIS memory P01h: B167 |      |      |      | Maximum duration of Module Pwr Up state.                                                                                                                       | 7     |
| Module Pwr Dn Max Duration         | See CMIS memory P01h: B167 |      |      |      | Maximum duration of Module Pwr Dn state.                                                                                                                       | 7     |
| I/O Timing for Squelch & Disable   |                            |      |      |      |                                                                                                                                                                |       |
| Rx Squelch Assert Time             |                            |      | 15   | ms   | Time from loss of Rx input signal until the squelched output condition is reached.                                                                             |       |
| Rx Squelch De-Assert Time          |                            |      | 15   | ms   | Time from resumption of Rx input signals until normal Rx output condition is reached.                                                                          |       |
| Tx Squelch Assert Time             |                            |      | 400  | ms   | Time from loss of Tx input signal until the squelched output condition is reached.                                                                             |       |
| Tx Squelch De-Assert Time          |                            |      | 10   | s    | Time from resumption of Tx input signal until the normal Tx output condition is reached.                                                                       |       |
| Rx Output Disable Assert Time      |                            |      | 100  | ms   | Time from Rx Output Disable bit set (value = 1b) until Rx output falls below 10% of nominal.                                                                   | 4     |

|                                         |  |  |     |    |                                                                                                                         |   |
|-----------------------------------------|--|--|-----|----|-------------------------------------------------------------------------------------------------------------------------|---|
| <b>Rx Output Disable De-Assert Time</b> |  |  | 100 | ms | Time from Rx Output Disable bit cleared to (value = 0b) until Rx output rises above 90% of nominal.                     | 4 |
| <b>Squelch Disable Assert Time</b>      |  |  | 100 | ms | This applies to Rx and Tx Squelch and is the time from bit set (value = 1b) until squelch functionality is disabled.    | 4 |
| <b>Squelch Disable De-Assert Time</b>   |  |  | 100 | ms | This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b) until squelch functionality is enabled. | 4 |

**Notes:**

1. "Power On" is defined as the instant when supply voltages reach and remain at or above the minimum level specified.
2. Measured from the rising edge of SDA during STOP sequence of write transaction.
3. RxLOS condition is defined as a Rx input power below threshold or DSP loss of signal.
4. Measured from Low to High SDA signal transition of the STOP condition of the write transaction.
5. Measured from Low to High SDA edge of the STOP condition of the write transaction.
6. Measured from the Low to High SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the write transaction until the IntL for the state change Vout:IntL=Vol.

**Optical Timing Characteristics**

| Parameter                        | Symbol | Min. | Max. | Unit | Conditions | Notes |
|----------------------------------|--------|------|------|------|------------|-------|
| <b>Tx Turn On Time</b>           |        |      | 10   | s    | Warm Start | 1     |
|                                  |        |      | 120  | s    | Cold Start |       |
| <b>Rx Acquisition Time</b>       |        |      | 30   | ms   | Warm Start |       |
|                                  |        |      | 120  | s    | Cold Start |       |
| <b>Tx/Rx Channel Tuning Time</b> |        | 10   | 30   | s    |            |       |

**Notes:**

1. Assumes the Tx/Rx laser is already tuned to the correct frequency.

## Pin Descriptions

| Pin | Logic       | Symbol       | Name/Description                                                                      | Plug Sequence | Notes |
|-----|-------------|--------------|---------------------------------------------------------------------------------------|---------------|-------|
| 1   |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 2   | CML-I       | Tx2-         | Transmitter Inverted Data Input.                                                      | 3             |       |
| 3   | CML-I       | Tx2+         | Transmitter Non-Inverted Data Input.                                                  | 3             |       |
| 4   |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 5   | CML-I       | Tx4-         | Transmitter Inverted Data Input.                                                      | 3             |       |
| 6   | CML-I       | Tx4+         | Transmitter Non-Inverted Data Input.                                                  | 3             |       |
| 7   |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 8   | LVTTL-I     | ModSelL      | Module Select.                                                                        | 3             |       |
| 9   | LVTTL-I     | ResetL       | Module Reset.                                                                         | 3             |       |
| 10  |             | VccRx        | +3.3V Receiver Power Supply.                                                          | 2             | 2     |
| 11  | LVC MOS-I/O | SCL          | 2-Wire Serial Interface Clock.                                                        | 3             |       |
| 12  | LVC MOS-I/O | SDA          | 2-Wire Serial Interface Data.                                                         | 3             |       |
| 13  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 14  | CML-O       | Rx3+         | Receiver Non-Inverted Data Output.                                                    | 3             |       |
| 15  | CML-O       | Rx3-         | Receiver Inverted Data Output.                                                        | 3             |       |
| 16  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 17  | CML-O       | Rx1+         | Receiver Non-Inverted Data Output.                                                    | 3             |       |
| 18  | CML-O       | Rx1-         | Receiver Inverted Data Output.                                                        | 3             |       |
| 19  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 20  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 21  | CML-O       | Rx2-         | Receiver Inverted Data Output.                                                        | 3             |       |
| 22  | CML-O       | Rx2+         | Receiver Non-Inverted Data Output.                                                    | 3             |       |
| 23  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 24  | CML-O       | Rx4-         | Receiver Inverted Data Output.                                                        | 3             |       |
| 25  | CML-O       | Rx4+         | Receiver Non-Inverted Data Output.                                                    | 3             |       |
| 26  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 27  | LVTTL-O     | ModPrsL      | Module Present.                                                                       | 3             |       |
| 28  | LVTTL-O     | IntL/RxLOSL  | Interrupt. Optionally configurable as RxLOSL via the management interface (CMIS).     | 3             |       |
| 29  |             | VccTx        | +3.3V Transmitter Power Supply.                                                       | 2             | 2     |
| 30  |             | Vcc1         | +3.3V Power Supply.                                                                   | 2             | 2     |
| 31  | LVTTL-I     | LPMode/TxDis | Low-Power Mode. Optionally configurable as TxDis via the management interface (CMIS). | 3             |       |
| 32  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 33  | CML-I       | Tx3+         | Transmitter Non-Inverted Data Input.                                                  | 3             |       |
| 34  | CML-I       | Tx3-         | Transmitter Inverted Data Input.                                                      | 3             |       |
| 35  |             | GND          | Module Ground.                                                                        | 1             | 1     |
| 36  | CML-I       | Tx1+         | Transmitter Non-Inverted Data Input.                                                  | 3             |       |
| 37  | CML-I       | Tx1-         | Transmitter Inverted Data Input.                                                      | 3             |       |
| 38  |             | GND          | Module Ground.                                                                        | 1             | 1     |

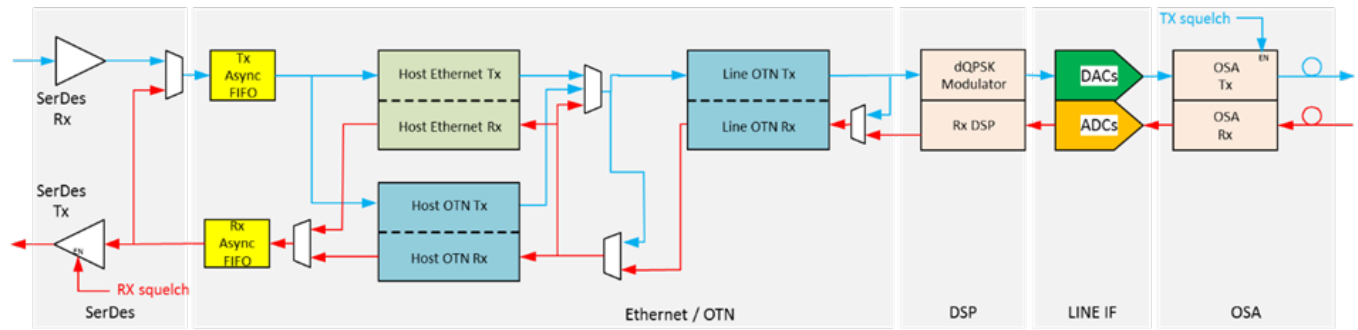
Notes:

- 1. GND is the symbol for signal and supply (power) common for the module. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- 2. VccRx, Vcc1, and VccTx are applied concurrently and may be internally connected within the module in any combination.
- 3. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, and 3. See figure below for pad locations.

Electrical Pad Layout



### Block Diagram



## Mechanical Specifications



# About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.

