OSFP224-1600GB-2XDR4-LRO-SKY

MSA 1.6T 2xDR4 PAM4 OSFP224-IHS Transceiver (SMF, 1310nm, 500m, 2xMPO-12, DOM, CMIS 5.3) LRO

Product Description

This MSA compliant OSFP224-IHS Transceiver provides 1600GBase-2xDR4 throughput up to 500m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO-12 connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

Features:

- OSFP Package
- 106GBaud Data Rate
- IHS (Close Top)
- Dual MPO-12 Optical Receptacle Connector
- Hot-Pluggable
- 3.3V Power Supply
- Up to 500m Transmission on Single-Mode Fiber
- CMIS 5.3 Compliant
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius

Applications:

- 16x100GBase Ethernet
- InfiniBand
- 2x800GBase Ethernet

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Ambient Temperature	Tstg	-40		85	°C	
Relative Humidity – Storage	RHs	0		95	%	1
Relative Humidity – Operating	RHo	0		85	%	1
Module Supply Voltage	Vcc	-0.5		3.6	V	

Notes:

1. Non-condensing.
2. Exceeding the Absolute Maximum Ratings may cause irreversible damage to the device. The device is not intended to be operated under the condition of simultaneous Absolute Maximum Ratings, a condition which may cause irreversible damage to the device.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Case Operating Temperature	Tc	0	25	70	°C	
Module Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption	PC			18	W	
PAM4 Signaling Rate Per Lane	SR		106.25		GBaud	1

Notes:

1. Range: ±100ppm.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter (Host Rx)						
Tx_Data Differential Input Voltage	VIN			880	mV	
Tx_Data Differential Input Impedance	ZIN		93		Ω	
Signaling Rate Per Lane	SR		106.25		GBaud	1
Receiver						
Rx_Data Differential Output Voltage	VOUT			TBD	mV	
Rx_Data Differential Output Impedance	ZOUT		93		Ω	2
Signaling Rate Per Lane	SR		106.25		GBaud	1

Notes:

1. Range: ±50ppm.
2. ±8%.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Rate Per Lane		106.25 ± 50ppm			GBd	
Laser Type		DFB+SiPho PIC				
Lane Wavelength	λ	1304.5		1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	POUT	-3.3		4	dBm	
Outer Optical Modulation Amplitude	OMAouter	-0.1		4.2	dBm	1
		-1+TDECQ		4.2	dBm	2
Transmitter and Dispersion Penalty Eye Closure for PAM4	TDECQ			3.4	dB	3
Optical Output with Tx Off Per Lane	POFF			-15	dBm	
Extinction Ratio	ER	3.5			dB	3
Transmitter Reflectance	RFL			-26	dB	
Receiver						
Signaling Rate Per Lane	SR	106.25 ± 50ppm			GBd	
Lane Wavelength	Λ	1304.5		1317.5	nm	
Receiver Sensitivity (OMAouter) Per Lane	SEN	-3.4		4.2	dBm	4, 6
		-4.3+TECQ		4.2	dBm	5, 6
Average Receiver Power Per Lane	PIN	-6.3		4	dBm	6
Damage Threshold Per Lane		5			dBm	
Receiver Reflectance	RFL			-26	dB	

Notes:

1. For TDECQ<0.9dB
2. For 0.9dB≤TDECQ≤3.4dB.
3. Test with SSPRQ pattern, the reference equalizer is 15-tap FFE.
4. For TECQ<0.9dB
5. For 0.9dB≤TECQ≤3.4dB.
6. PAM4 Signaling rate per lane 106.25GBaud, $6.4E^{-5}$ and PRBS 2^{31}-1.

Pin Descriptions

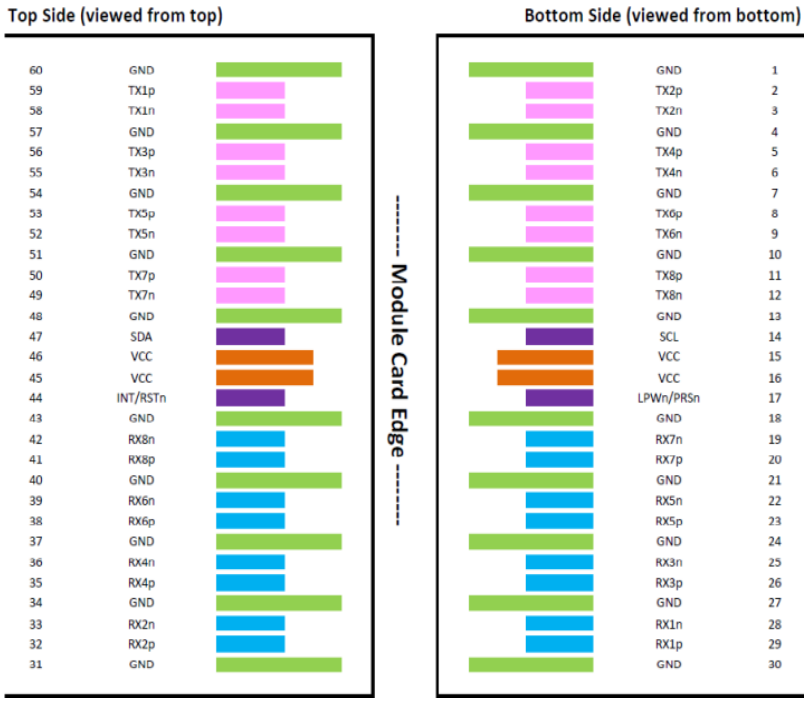
Pin	Logic	Symbol	Name/Description	Direction	Plug Sequence	Notes
1		GND	Module Ground.		1	
2	CML-I	TX2P	CH2 Transmitter Date Non-Inverted.	Input from Host	3	
3	CML-I	TX2N	CH2 Transmitter Date Inverted.	Input from Host	3	
4		GND	Module Ground.		1	
5	CML-I	TX4P	CH4 Transmitter Date Non-Inverted.	Input from Host	3	
6	CML-I	TX4N	CH4 Transmitter Date Inverted.	Input from Host	3	
7		GND	Module Ground.		1	
8	CML-I	TX6P	CH6 Transmitter Date Non-Inverted.	Input from Host	3	
9	CML-I	TX6N	CH6 Transmitter Date Inverted.	Input from Host	3	
10		GND	Module Ground.		1	
11	CML-I	TX8P	CH8 Transmitter Date Non-Inverted.	Input from Host	3	
12	CML-I	TX8N	CH8 Transmitter Date Inverted.	Input from Host	3	
13		GND	Module Ground.		1	
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	Bi-Directional	3	1
15		Vcc	+3.3V Power Supply.	Power from Host	2	
16		Vcc	+3.3V Power Supply.	Power from Host	2	
17	Multi-Level	LPWN/PRSN	Low-Power Mode/Module Present.	Bi-Directional	3	2
18		GND	Module Ground.		1	
19	CML-O	RX7N	CH7 Receiver Date Inverted.	Output to Host	3	
20	CML-O	RX7P	CH7 Receiver Date Non-Inverted.	Output to Host	3	
21		GND	Module Ground.		1	
22	CML-O	RX5N	CH5 Receiver Date Inverted.	Output to Host	3	
23	CML-O	RX5P	CH5 Receiver Date Non-Inverted.	Output to Host	3	
24		GND	Module Ground.		1	
25	CML-O	RX3N	CH3 Receiver Date Inverted.	Output to Host	3	
26	CML-O	RX3P	CH3 Receiver Date Non-Inverted.	Output to Host	3	
27		GND	Module Ground.		1	
28	CML-O	RX1N	CH1 Receiver Date Inverted.	Output to Host	3	
29	CML-O	RX1P	CH1 Receiver Date Non-Inverted.	Output to Host	3	
30		GND	Module Ground.		1	
31		GND	Module Ground.		1	
32	CML-O	RX2P	CH2 Receiver Date Non-Inverted.	Output to Host	3	
33	CML-O	RX2N	CH2 Receiver Date Inverted.	Output to Host	3	
34		GND	Module Ground.		1	
35	CML-O	RX4P	CH4 Receiver Date Non-Inverted.	Output to Host	3	
36	CML-O	RX4N	CH4 Receiver Date Inverted.	Output to Host	3	

37		GND	Module Ground.		1	
38	CML-O	RX6P	CH6 Receiver Date Non-Inverted.	Output to Host	3	
39	CML-O	RX6N	CH6 Receiver Date Inverted.	Output to Host	3	
40		GND	Module Ground.		1	
41	CML-O	RX8P	CH8 Receiver Date Non-Inverted.	Output to Host	3	
42	CML-O	RX8N	CH8 Receiver Date Inverted.	Output to Host	3	
43		GND	Module Ground.		1	
44	Multi-Level	INT/RSTN	Module Interrupt/Module Reset.	Bi-Directional	3	3
45		Vcc	+3.3V Power Supply.	Power from Host	2	
46		Vcc	+3.3V Power Supply.	Power from Host	2	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	Bi-Directional	3	1
48		GND	Module Ground.		1	
49	CML-I	TX7N	CH7 Transmitter Date Inverted.	Input from Host	3	
50	CML-I	TX7P	CH7 Transmitter Date Non-Inverted.	Input from Host	3	
51		GND	Module Ground.		1	
52	CML-I	TX5N	CH5 Transmitter Date Inverted.	Input from Host	3	
53	CML-I	TX5P	CH5 Transmitter Date Non-Inverted.	Input from Host	3	
54		GND	Module Ground.		1	
55	CML-I	TX3N	CH3 Transmitter Date Inverted.	Input from Host	3	
56	CML-I	TX3P	CH3 Transmitter Date Non-Inverted.	Input from Host	3	
57		GND	Module Ground.		1	
58	CML-I	TX1N	CH1 Transmitter Date Inverted.	Input from Host	3	
59	CML-I	TX1P	CH1 Transmitter Date Non-Inverted.	Input from Host	3	
60		GND	Module Ground.		1	

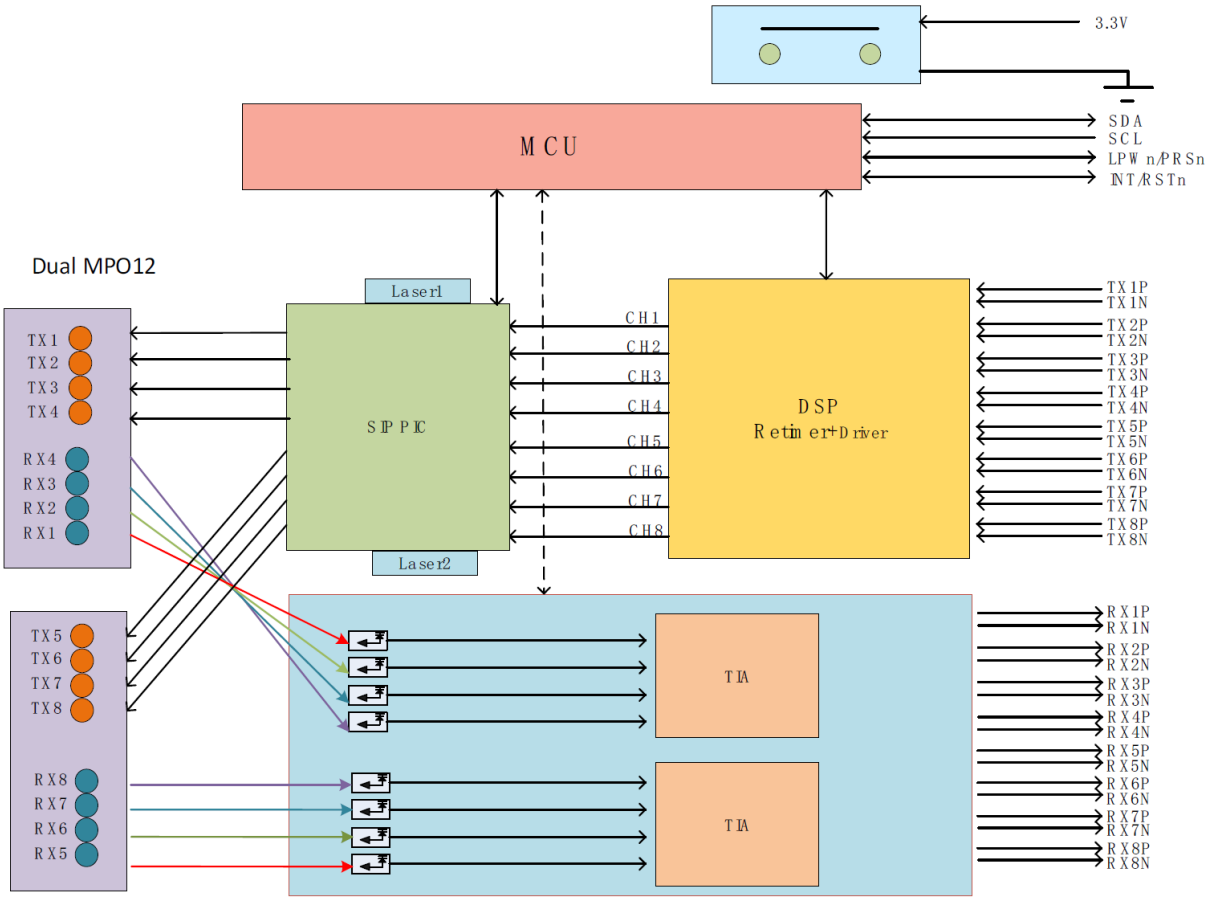
Notes:

1. Open-drain with pull-up resistor on host.
2. LPWn/PRSn is a dual function signal that allows the host to signal Low-Power Mode and for the module to indicate that the module is present.
3. INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module.

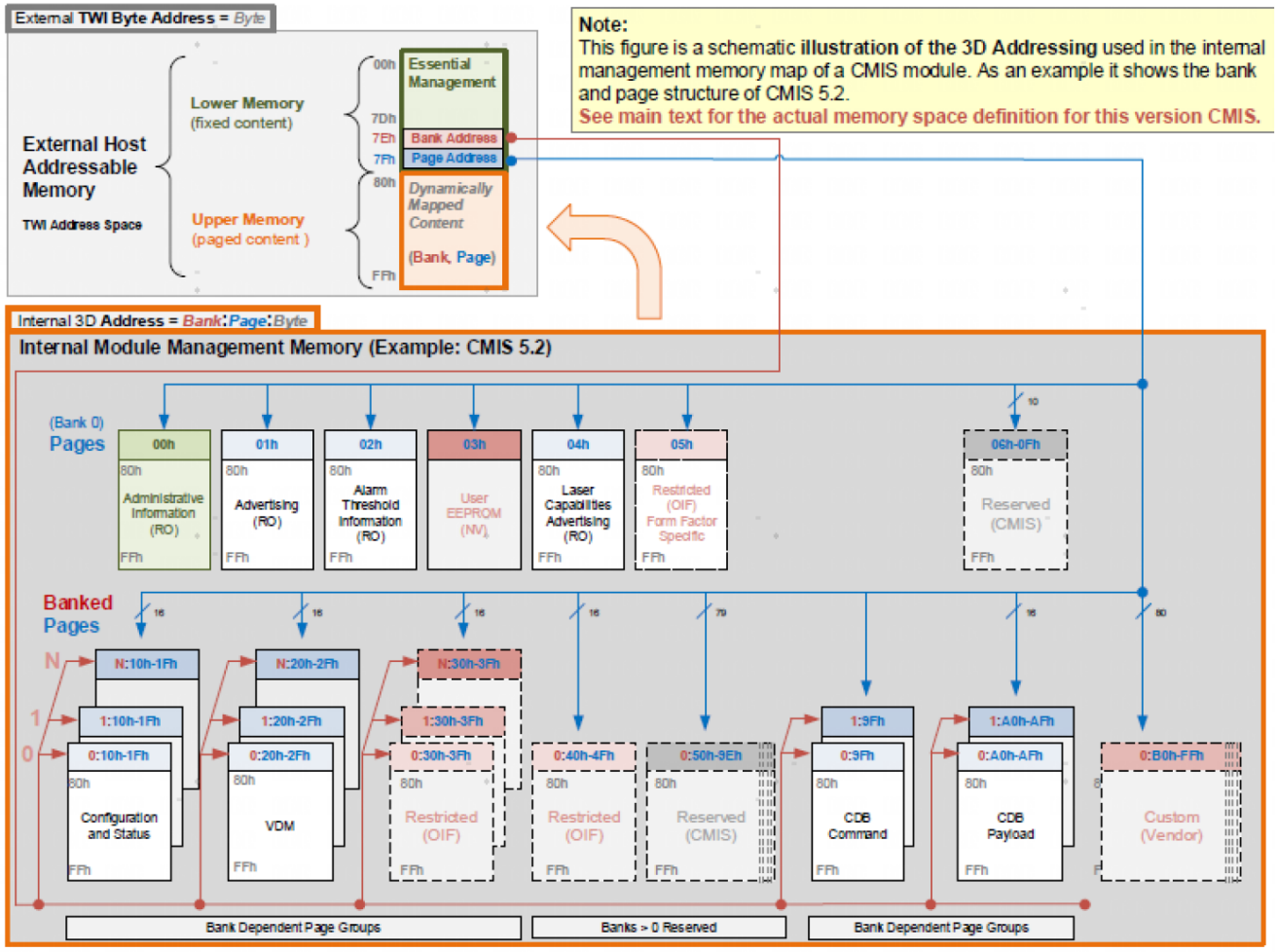
Electrical Pad Layout



Block Diagram



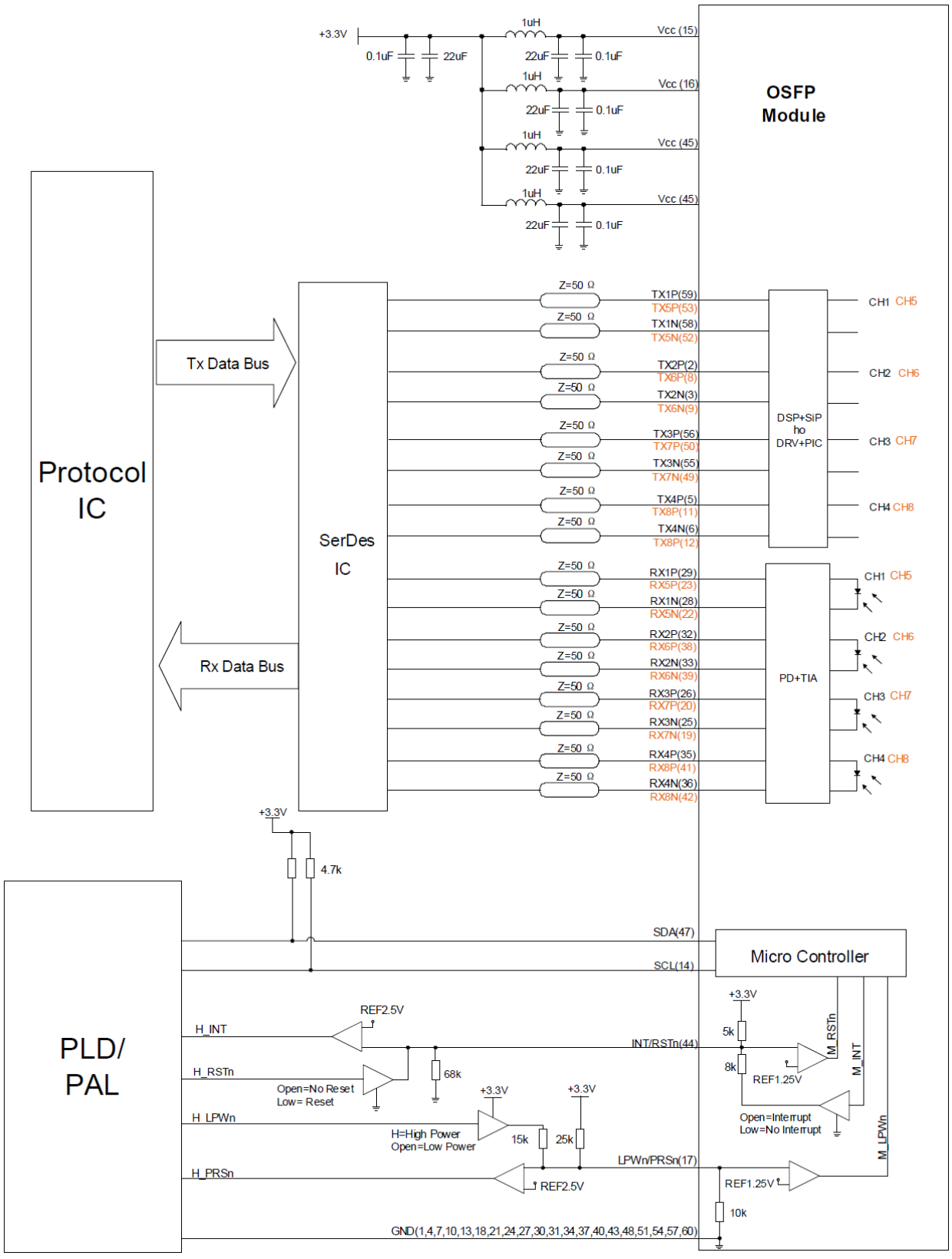
2-Wire Serial Memory Map



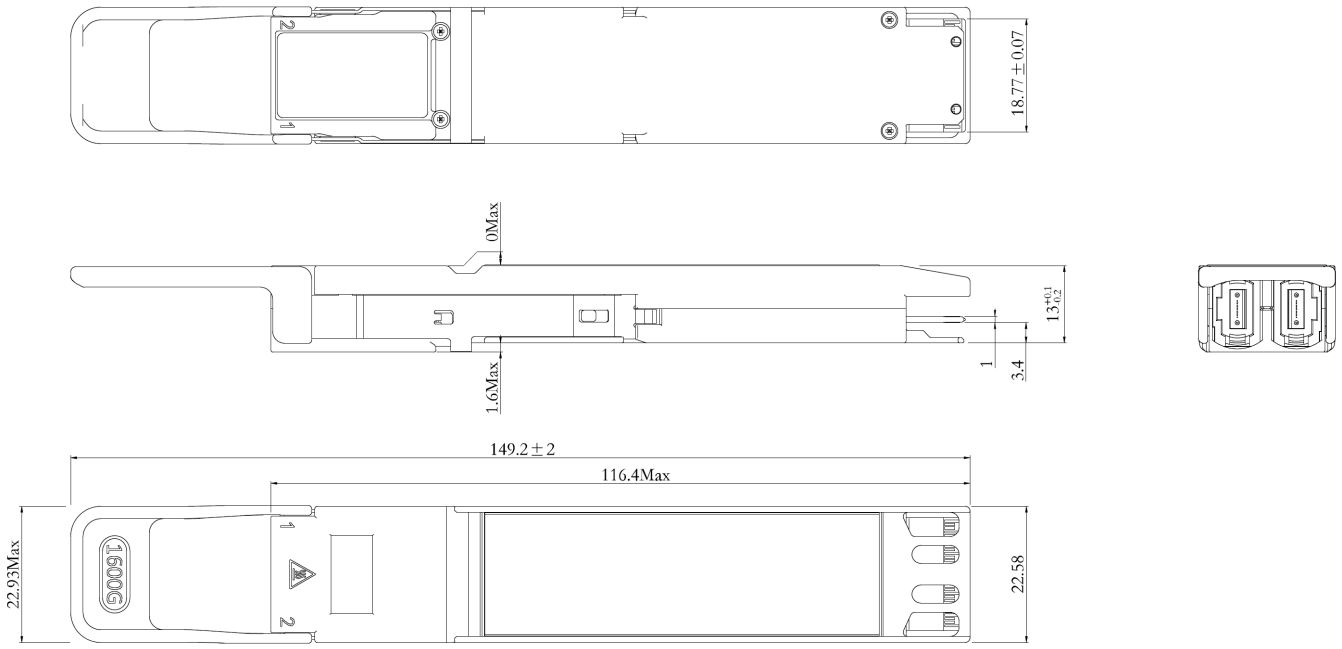
Notes:

1. For detailed definitions of the registers, please refer to Common Management Interface Specifications for 8/16x Pluggable Transceivers R5.3.

Host Board


+3.3V
1uH
0.1uF
22uF
Vcc (15)
Vcc (16)
Vcc (45)
Vcc (45)
OSFP Module
Protocol IC
Tx Data Bus
Rx Data Bus
SerDes IC
Z=50 Ω
TX1P(59)
TX5P(53)
TX1N(58)
TX5N(52)
TX2P(2)
TX6P(8)
TX2N(3)
TX6N(9)
TX3P(56)
TX7P(50)
TX3N(55)
TX7N(49)
TX4P(5)
TX8P(11)
TX4N(6)
TX8P(12)
DSP+SiPho DRV+PIC
CH1 CH5
CH2 CH6
CH3 CH7
CH4 CH8
RX1P(29)
RX5P(23)
RX1N(28)
RX5N(22)
RX2P(32)
RX6P(38)
RX2N(33)
RX6N(39)
RX3P(26)
RX7P(20)
RX3N(25)
RX7N(19)
RX4P(35)
RX8P(41)
RX4N(36)
RX8N(42)
PD+TIA
4.7k
PLD/ PAL
SDA(47)
SCL(14)
Micro Controller
H_INT
REF2.5V
INT/RSTn(44)
H_RSTn
Open=No Reset
Low= Reset
68k
5k
8k
REF1.25V
M_RSTn
M_INT
Open=Interrupt
Low=No Interrupt
H_LPWn
H=High Power
Open=Low Power
15k
25k
M_LPWn
LPWn/PRSn(17)
H_PRSn
REF2.5V
10k
GND(1,4,7,10,13,18,21,24,27,30,31,34,37,40,43,48,51,54,57,60)

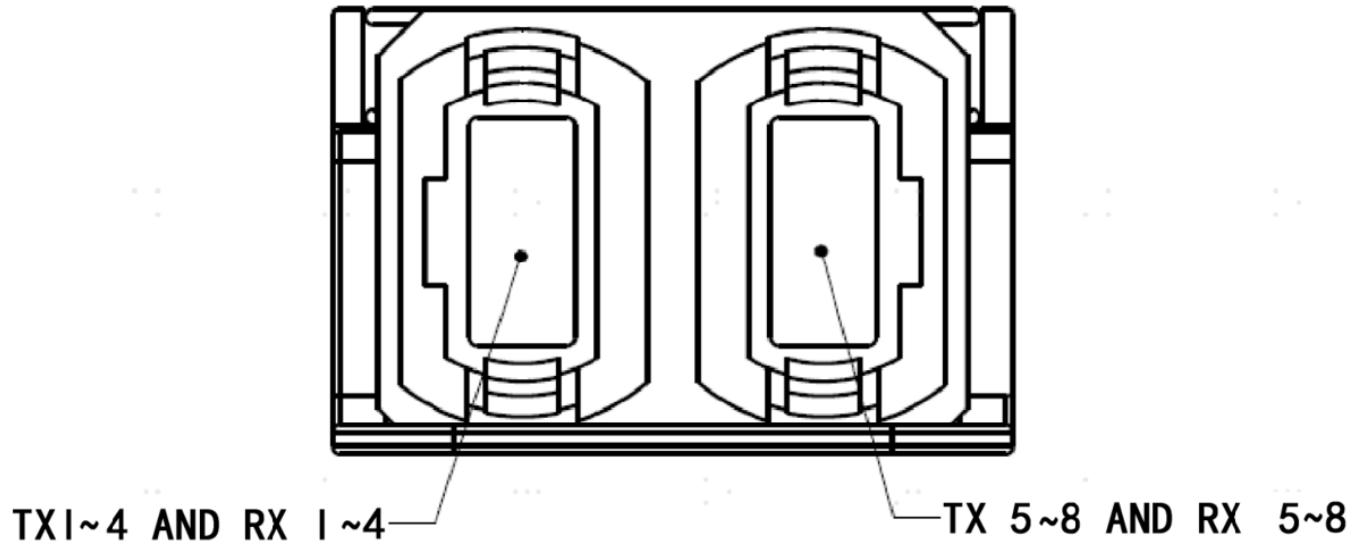
Mechanical Specifications



Notes:

1. Tolerance: ±0.1mm.
2. Others according with OSFP MSA.
3. Optical port according with Fiber Connector Specifications.

Optical Lane Assignment



About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.