



OSFP-QDD-CVR-SKY

MSA Compliant 800GBase-Converter OSFP-IHS Transceiver (OSFP-IHS to QSFP-DD Converter)

Product Description

This MSA compliant OSFP-IHS to QSFP-DD converter provides conversion from OSFP-IHS to QSFP-DD form factors. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that it will integrate into your network seamlessly. It is built to meet or exceed the specifications of MSA Compliant, as well as to comply with MSA (Multi-Source Agreement) standards to ensure seamless network integration. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

Features:

- Data Rates: 56Gbps Per Lane or 112Gbps Per Lane
- Compliant with IEEE802.3cd (400GBASE-CR8, 200GBASE-CR4)
- Compliant with IEEE802.3ck (800GBASE-CR8, 400GBASE-CR4)
- Connector Compliant with OSFP Octal Small Form Factor Pluggable Module - OSFP MSA and QSFP-DD MSA Standard
- Standard Power Consumption: 16W
- Compliant with IEEE802.3bj (200GBASE-CR8, 100GBASE-CR4)
- Operating Temperature: 0 to 70 Celsius
- Low-Power Consumption: 0.5W
- RoHS Compliant and Lead-Free



Applications:

- 800GBase Ethernet

For your product safety, please read the following information carefully before any manipulation of the transceiver:



ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	Tc	0		70	°C	
Storage Temperature	Tstg	0		70	°C	
Relative Humidity (Non-Condensing)	RH			85	%	
Supply Voltage	Vcc	3.15		3.45	V	
Power Consumption	PC			0.5	W	
Characteristic Impedance	Im	90		110	Ω	
Data Rate	DR	25		112	Gbps	

OSFP Pin Descriptions

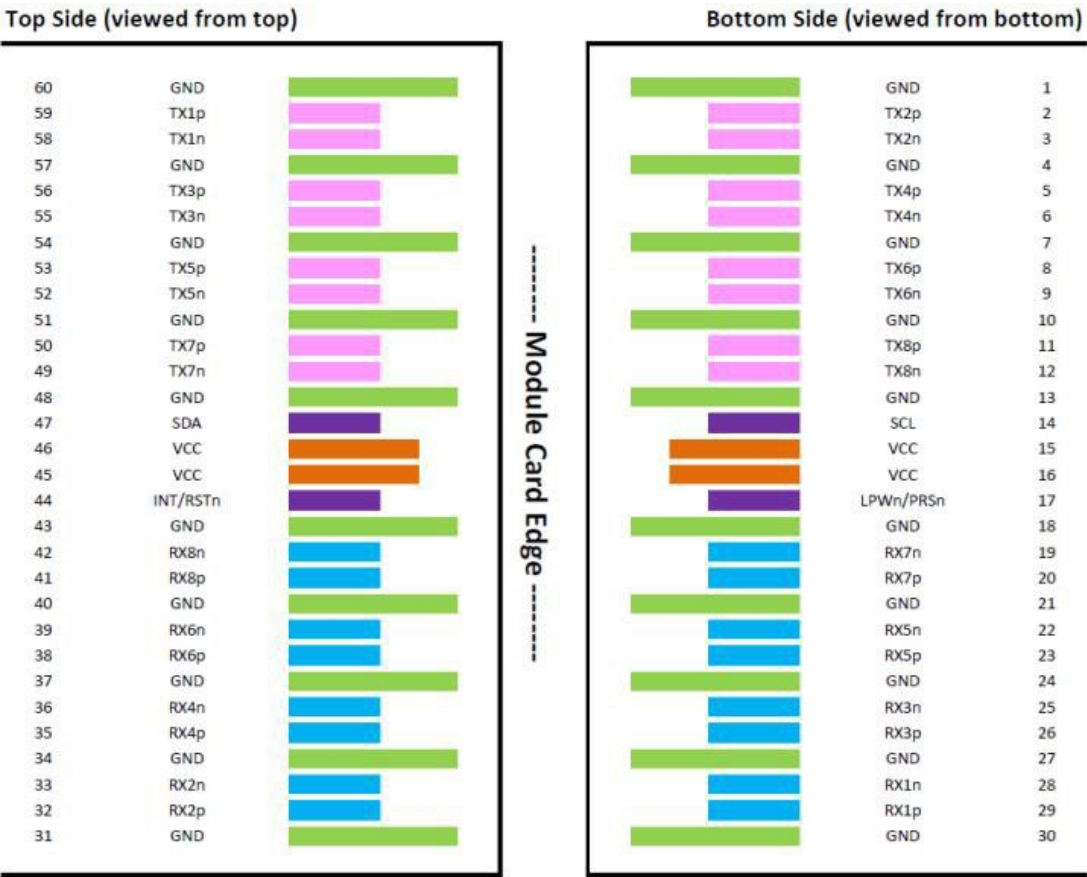
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2+	Non-Inverted Transmitter Data.	3	
3	CML-I	Tx2-	Inverted Transmitter Data.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4+	Non-Inverted Transmitter Data.	3	
6	CML-I	Tx4-	Inverted Transmitter Data.	3	
7		GND	Module Ground.	1	1
8	CML-I	Tx6+	Non-Inverted Transmitter Data.	3	
9	CML-I	Tx6-	Inverted Transmitter Data.	3	
10		GND	Module Ground.	1	1
11	CML-I	Tx8+	Non-Inverted Transmitter Data.	3	
12	CML-I	Tx8-	Inverted Transmitter Data.	3	
13		GND	Module Ground.	1	1
14	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3	2
15		Vcc	+3.3V Power.	2	
16		Vcc	+3.3V Power.	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	3	
18		GND	Module Ground.	1	1
19	CML-O	Rx7-	Inverted Receiver Data.	3	
20	CML-O	Rx7+	Non-Inverted Receiver Data.	3	
21		GND	Module Ground.	1	1
22	CML-O	Rx5-	Inverted Receiver Data.	3	
23	CML-O	Rx5+	Non-Inverted Receiver Data.	3	
24		GND	Module Ground.	1	1

25	CML-O	Rx3-	Inverted Receiver Data.	3	
26	CML-O	Rx3+	Non-Inverted Receiver Data.	3	
27		GND	Module Ground.	1	1
28	CML-O	Rx1-	Inverted Receiver Data.	3	
29	CML-O	Rx1+	Non-Inverted Receiver Data.	3	
30		GND	Module Ground.	1	1
31		GND	Module Ground.	1	1
32	CML-O	Rx2+	Non-Inverted Receiver Data.	3	
33	CML-O	Rx2-	Inverted Receiver Data.	3	
34		GND	Module Ground.	1	1
35	CML-O	Rx4+	Non-Inverted Receiver Data.	3	
36	CML-O	Rx4-	Inverted Receiver Data.	3	
37		GND	Module Ground.	1	1
38	CML-O	Rx6+	Non-Inverted Receiver Data.	3	
39	CML-O	Rx6-	Inverted Receiver Data.	3	
40		GND	Module Ground.	1	1
41	CML-O	Rx8+	Non-Inverted Receiver Data.	3	
42	CML-O	Rx8-	Inverted Receiver Data.	3	
43		GND	Module Ground.	1	1
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	3	
45		Vcc	+3.3V Power.	2	
46		Vcc	+3.3V Power.	2	
47	LVC MOS-I/O	SCL	2-Wire Serial interface Data.	3	2
48		GND	Module Ground.	1	1
49	CML-I	Tx7-	Inverted Transmitter Data.	3	
50	CML-I	Tx7+	Non-Inverted Transmitter Data.	3	
51		GND	Module Ground.	1	1
52	CML-I	Tx5-	Inverted Transmitter Data.	3	
53	CML-I	Tx5+	Non-Inverted Transmitter Data.	3	
54		GND	Module Ground.	1	1
55	CML-I	Tx3-	Inverted Transmitter Data.	3	
56	CML-I	Tx3+	Non-Inverted Transmitter Data.	3	
57		GND	Module Ground.	1	1
58	CML-I	Tx1-	Inverted Transmitter Data.	3	
59	CML-I	Tx1+	Non-Inverted Transmitter Data.	3	
60		GND	Module Ground.	1	1

Notes:

- 1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module, and all module voltages are referenced to this potential unless otherwise noted.
- 2. Open-drain with pull-up resistor on the host.

Electrical Pad Layout



QSFP-DD Pin Descriptions

Pin	Logic	Symbol	Name/Description		Notes
1		GND	Module Ground.	1B	1
2	CML-I	Tx2-	Inverted Transmitter Data Input.	3B	
3	CML-I	Tx2+	Non-Inverted Transmitter Data Input.	3B	
4		GND	Module Ground.	1B	1
5	CML-I	Tx4-	Inverted Transmitter Data Input.	3B	
6	CML-I	Tx4+	Non-Inverted Transmitter Data Input.	3B	
7		GND	Module Ground.	1B	1
8	LVTTTL-I	ModSelL	Module Select.	3B	
9	LVTTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Receiver Power Supply.	2B	2
11	LVC MOS- I/O	SCL	2-Wire Serial Interface Clock.	3B	
12	LVC MOS- I/O	SDA	2-Wire Serial Interface Data.	3B	
13		GND	Module Ground.	1B	1
14	CML-O	Rx3+	Non-Inverted Receiver Data Output.	3B	
15	CML-O	Rx3-	Inverted Receiver Data Output.	3B	
16		GND	Module Ground.	1B	1
17	CML-O	Rx1+	Non-Inverted Receiver Data Output.	3B	
18	CML-O	Rx1-	Inverted Receiver Data Output.	3B	
19		GND	Module Ground.	1B	1
20		GND	Module Ground.	1B	1
21	CML-O	Rx2-	Inverted Receiver Data Output.	3B	
22	CML-O	Rx2+	Non-Inverted Receiver Data Output.	3B	
23		GND	Module Ground.	1B	1
24	CML-O	Rx4-	Inverted Receiver Data Output.	3B	
25	CML-O	Rx4+	Non-Inverted Receiver Data Output.	3B	
26		GND	Module Ground.	1B	1
27	LVTTTL-O	ModPrsL	Module Present.	3B	
28	LVTTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Transmitter Power Supply.	2B	2
30		Vcc1	+3.3V Power Supply.	2B	2
31	LVTTTL-I	LPMode	Low-Power Mode.	3B	
32		GND	Module Ground.	1B	1
33	CML-I	Tx3+	Non-Inverted Transmitter Data Input.	3B	
34	CML-I	Tx3-	Inverted Transmitter Data Input.	3B	
35		GND	Module Ground.	1B	1
36	CML-I	Tx1+	Non-Inverted Transmitter Data Input.	3B	
37	CML-I	Tx1-	Inverted Transmitter Data Input.	3B	
38		GND	Module Ground.	1B	1
39		GND	Module Ground.	1A	1
40	CML-I	Tx6-	Inverted Transmitter Data Input.	3A	

41	CML-I	Tx6+	Non-Inverted Transmitter Data Input.	3A	
42		GND	Module Ground.	1A	1
43	CML-I	Tx8-	Inverted Transmitter Data Input.	3A	
44	CML-I	Tx8+	Non-Inverted Transmitter Data Input.	3A	
45		GND	Module Ground.	1A	1
46		Reserved	For Future Use.	3A	3
47		VS1	Module Vendor-Specific 1.	3A	3
48		VccRx1	+3.3V Receiver Power Supply.	2A	2
49		VS2	Module Vendor-Specific 2.	3A	3
50		VS3	Module Vendor-Specific 3.	3A	3
51		GND	Module Ground.	1A	1
52	CML-O	Rx7+	Non-Inverted Receiver Data Output.	3A	
53	CML-O	Rx7-	Inverted Receiver Data Output.	3A	
54		GND	Module Ground.	1A	1
55	CML-O	Rx5+	Non-Inverted Receiver Data Output.	3A	
56	CML-O	Rx5-	Inverted Receiver Data Output.	3A	
57		GND	Module Ground.	1A	1
58		GND	Module Ground.	1A	1
59	CML-O	Rx6-	Inverted Receiver Data Output.	3A	
60	CML-O	Rx6+	Non-Inverted Receiver Data Output.	3A	
61		GND	Module Ground.	1A	1
62	CML-O	Rx8-	Inverted Receiver Data Output.	3A	
63	CML-O	Rx8+	Non-Inverted Receiver Data Output.	3A	
64		GND	Module Ground.	1A	1
65		NC	Not Connected.	3A	3
66		Reserved	For Future Use.	3A	3
67		VccTx1	+3.3V Transmitter Power Supply.	2A	2
68		Vcc2	+3.3V Power Supply.	2A	2
69		Reserved	For Future Use.	3A	3
70		GND	Module Ground.	1A	1
71	CML-I	Tx7+	Non-Inverted Transmitter Data Input.	3A	
72	CML-I	Tx7-	Inverted Transmitter Data Input.	3A	
73		GND	Module Ground.	1A	1
74	CML-I	Tx5+	Non-Inverted Transmitter Data Input.	3A	
75	CML-I	Tx5-	Inverted Transmitter Data Input.	3A	
76		GND	Module Ground.	1A	1

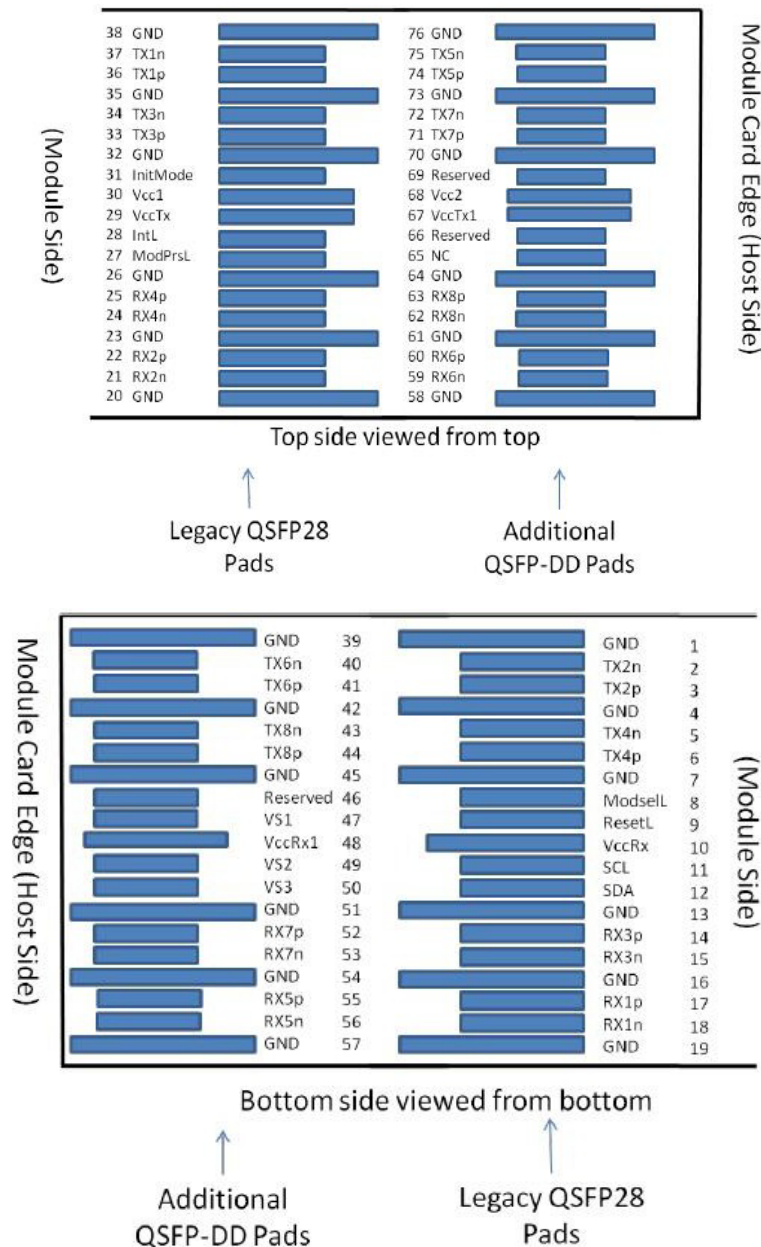
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1,

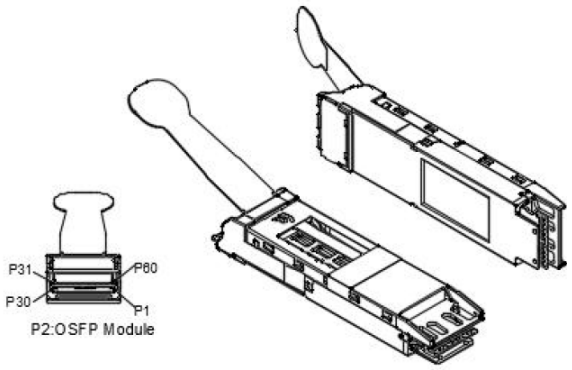
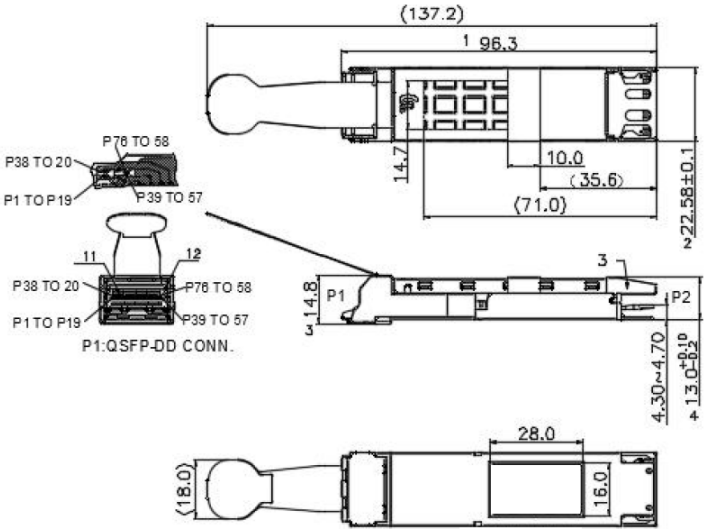
Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

3. All Vendor-Specific, Reserved, and Not Connected pins may be terminated with 50Ω to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break, contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Electrical Pad Layout



Mechanical Specifications



About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.

