



## OSFP-800GB-AEC-1M-NV-SKY

Nvidia® Compatible 800GBase-AEC OSFP to OSFP Active Electrical Cable (AEC, 1m, CMIS 5.0)

### Product Description

This is a Nvidia® compatible 800GBase-AEC OSFP to OSFP active electrical cable that operates over active copper with a maximum reach of 1.0m (3.3ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active electrical cable is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

### Features:

- 8-Lane Active Transceiver, Supports Data Rates up to 800Gbps
- Hot-Pluggable OSFP Type 1 Form Factor, MSA Compliant
- 8x106.25Gbps Tx and 8x106.25Gbps Rx Parallel Channels
- PAM4 Encoding
- CMIS 5.1
- Power Consumption: 8.0W Per Cable End
- Operating Temperature Range: 0 to 70 Celsius
- Single 3.3V Power Supply
- RoHS Compliant and Lead-Free



### Applications:

- 800GBase Ethernet

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*For your product safety, please read the following information carefully before any manipulation of the transceiver:*



#### **ESD**

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



#### **LASER SAFETY**

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

*The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.*

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General Specifications

| Parameter                   | Symbol | Min. | Typ.   | Max.               | Unit | Notes |
|-----------------------------|--------|------|--------|--------------------|------|-------|
| Storage Temperature         | Tstg   | -40  |        | 85                 | °C   |       |
| Operating Case Temperature  | Tc     | 0    |        | 70                 | °C   |       |
| Relative Operating Humidity | RH     | 5    |        | 85                 | %    |       |
| Bend Radius                 |        | 3    |        |                    | cm   |       |
| Data Rate Per Channel       | DR     |      | 53.125 |                    | GBd  |       |
| Aggregate Bit Rate          | BRAVE  |      | 800    |                    | Gbps |       |
| Lane Bit Rate               | BRLANE |      | 106.25 |                    | Gbps | 1     |
| Label Bit Tolerance         |        | -100 |        | 100                | ppm  |       |
| Bit Error Ratio             | BER    |      |        | 2.4E <sup>-4</sup> |      | 2     |
| 2-Wire Serial Interface     | I2C    |      | 400    | 1000               | kHz  | 3     |

Notes:

- 1. PAM4.
- 2. Pre-FEC.
- 3. Timing per CMIS 5.x.

Physical Characteristics

| Parameter       | Symbol                              | Min. | Typ. | Max. | Unit | Notes |
|-----------------|-------------------------------------|------|------|------|------|-------|
| Length          | L                                   |      |      | 1    | M    |       |
| AWG             |                                     |      | 30   |      | AWG  |       |
| Jacket Material | Plastic Braided Mesh Technology Net |      |      |      |      |       |

## Electrical Specifications

| Parameter                                         | Symbol        | Min.                          | Typ. | Max.    | Unit  | Notes |
|---------------------------------------------------|---------------|-------------------------------|------|---------|-------|-------|
| Supply Voltage                                    | Vcc           | 3.13                          | 3.3  | 3.47    | V     |       |
| Power Dissipation Per End                         | PD            |                               | 6.5  | 8.0     | W     |       |
| ESD Rating High-Speed Signal Pins                 | VESD_IO       | -1                            |      | 1       | kV    |       |
| ESD Rating All Pins Except High-Speed Signal Pins | VESD          | -2                            |      | 2       | kV    |       |
| SCL and SDA Outputs                               | VOL           | 0                             |      | 0.4     | V     |       |
| SCL and SDA Inputs                                | VIL           | -0.3                          |      | Vcc*0.3 | V     |       |
|                                                   | VIH           | Vcc*0.7                       |      | Vcc+0.5 | V     |       |
| INT/RSTn                                          | H_Vref_INT    | 2.475                         | 2.5  | 2.525   | V     |       |
|                                                   | M_Vref_RSTn   | 1.238                         | 1.25 | 1.263   | V     |       |
|                                                   | V_INT/RSTN_1  | 0                             | 0    | 1       | V     |       |
|                                                   | V_INT/RSTN_2  | 0                             | 0    | 1       | V     |       |
|                                                   | V_INT/RSTN_3  | 1.5                           | 1.9  | 2.25    | V     |       |
|                                                   | V_INT/RSTN_4  | 2.75                          | 3.0  | 3.465   | V     |       |
| LPWn/PRSn                                         | H_Vref_PRSn   | 2.475                         | 2.5  | 2.525   | V     |       |
|                                                   | M_Vref_LPWn   | 1.238                         | 1.25 | 1.263   | V     |       |
|                                                   | V_LPWn/PRSn_1 | 0                             | 0.95 | 1.1     | V     |       |
|                                                   | V_LPWn/PRSn_2 | 1.4                           | 1.7  | 2.25    | V     |       |
|                                                   | V_LPWn/PRSn_3 | 2.75                          | 3.3  | 3.465   | V     |       |
| Transmitter                                       |               |                               |      |         |       |       |
| Single-Ended Input Voltage                        |               | -0.35                         |      | 2.85    | V     |       |
| Differential Pk-Pk Input Voltage                  | VIN,pp        | 900                           |      |         | mVp-p |       |
| Differential Input Impedance                      | ZIN           | 80                            | 100  | 120     | Ω     |       |
| Differential to Common-Mode Return Loss           | SCD11         | IEEE802.3ck_Equation (120G-2) |      |         | dB    |       |
| Effective Return Loss (ERL)                       |               |                               |      | 8.5     | dB    |       |
| Differential Termination Mismatch                 |               |                               |      | 10      | %     |       |
| Receiver                                          |               |                               |      |         |       |       |
| Single-Ended Output Voltage                       |               | -0.35                         |      | 2.85    | V     |       |
| AC Common-Mode Voltage                            |               |                               |      | 17.5    | mV    |       |
| Differential Output Voltage Swing                 | VOUT,pp       |                               |      | 900     | mVp-p |       |
| Differential Output Impedance                     | ZOUT          | 80                            | 100  | 120     | Ω     |       |
| Common-Mode to Differential Return Loss           | SCD11         | IEEE802.3ck_Equation (120G-1) |      |         | dB    |       |
| Effective Return Loss (ERL)                       |               | 8.5                           |      |         | dB    |       |
| Differential Termination Mismatch                 |               |                               |      | 10      | !     |       |
| Transition Time (20-80%)                          | Tr/Tf         | 8.5                           |      |         | ps    |       |

## Pin Descriptions

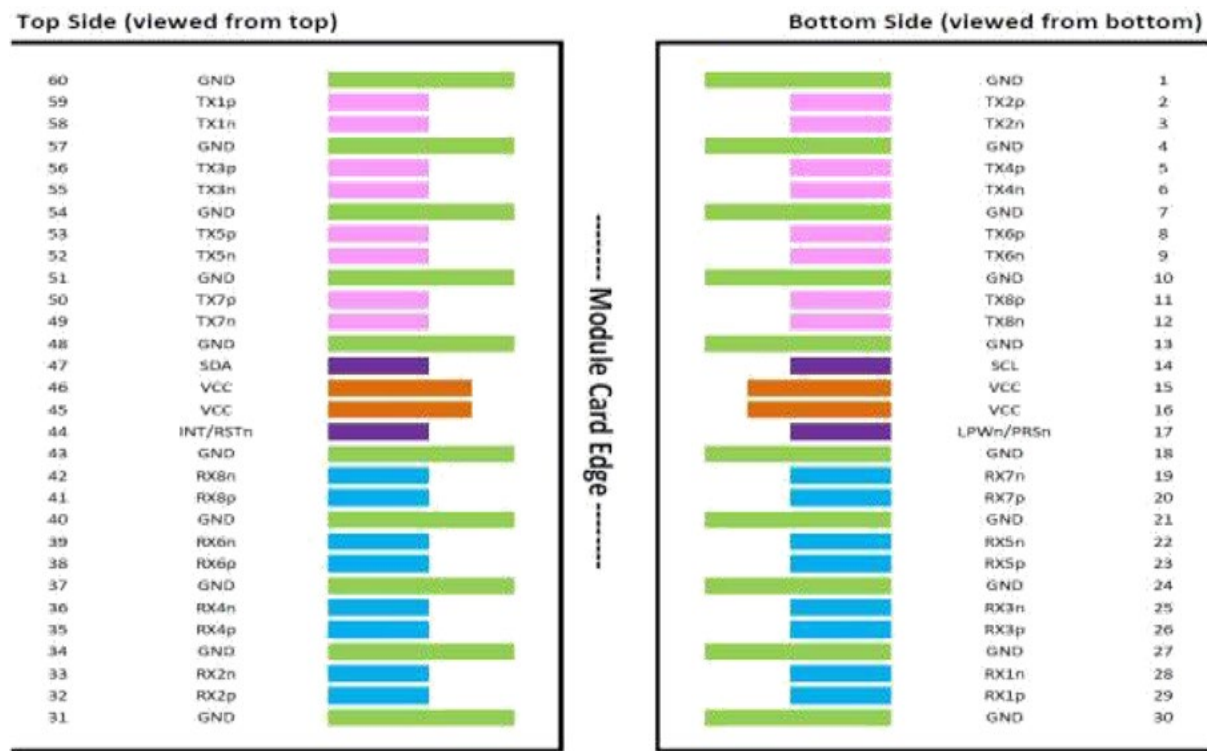
| Pin | Symbol    | Name/Description               | Logic       | Plug Sequence | Direction        | Notes |
|-----|-----------|--------------------------------|-------------|---------------|------------------|-------|
| 1   | GND       | Module Ground.                 |             | 1             |                  |       |
| 2   | Tx2+      | Transmitter Data Non-Inverted. | CML-I       | 3             | Input from Host  |       |
| 3   | Tx2-      | Transmitter Data Inverted.     | CML-I       | 3             | Input from Host  |       |
| 4   | GND       | Module Ground.                 |             | 1             |                  |       |
| 5   | Tx4+      | Transmitter Data Non-Inverted. | CML-I       | 3             | Input from Host  |       |
| 6   | Tx4-      | Transmitter Data Inverted.     | CML-I       | 3             | Input from Host  |       |
| 7   | GND       | Module Ground.                 |             | 1             |                  |       |
| 8   | Tx6+      | Transmitter Data Non-Inverted. | CML-I       | 3             | Input from Host  |       |
| 9   | Tx6-      | Transmitter Data Inverted.     | CML-I       | 3             | Input from Host  |       |
| 10  | GND       | Module Ground.                 |             | 1             |                  |       |
| 11  | Tx8+      | Transmitter Data Non-Inverted. | CML-I       | 3             | Input from Host  |       |
| 12  | Tx8-      | Transmitter Data Inverted.     | CML-I       | 3             | Input from Host  |       |
| 13  | GND       | Module Ground.                 |             | 1             |                  |       |
| 14  | SCL       | 2-Wire Serial Interface Clock. | LVCMOS-I/O  | 3             | Bi-Directional   | 1     |
| 15  | Vcc       | +3.3V Power.                   |             | 2             | Power from Host  |       |
| 16  | Vcc       | +3.3V Power.                   |             | 2             | Power from Host  |       |
| 17  | LPWn/PRSn | Low-Power Mode/Module Present. | Multi-Level | 3             | Bi-Directional   | 2     |
| 18  | GND       | Module Ground.                 |             | 1             |                  |       |
| 19  | Rx7-      | Receiver Data Inverted.        | CML-O       | 3             | Output from Host |       |
| 20  | Rx7+      | Receiver Data Non-Inverted.    | CML-O       | 3             | Output from Host |       |
| 21  | GND       | Module Ground.                 |             | 1             |                  |       |
| 22  | Rx5-      | Receiver Data Inverted.        | CML-O       | 3             | Output from Host |       |
| 23  | Rx5+      | Receiver Data Non-Inverted.    | CML-O       | 3             | Output from Host |       |
| 24  | GND       | Module Ground.                 |             | 1             |                  |       |
| 25  | Rx3-      | Receiver Data Inverted.        | CML-O       | 3             | Output from Host |       |
| 26  | Rx3+      | Receiver Data Non-Inverted.    | CML-O       | 3             | Output from Host |       |
| 27  | GND       | Module Ground.                 |             | 1             |                  |       |
| 28  | Rx1-      | Receiver Data Inverted.        | CML-O       | 3             | Output from Host |       |
| 29  | Rx1+      | Receiver Data Non-Inverted.    | CML-O       | 3             | Output from Host |       |
| 30  | GND       | Module Ground.                 |             | 1             |                  |       |
| 31  | GND       | Module Ground.                 |             | 1             |                  |       |
| 32  | Rx2+      | Receiver Data Non-Inverted.    | CML-O       | 3             | Output from Host |       |
| 33  | Rx2-      | Receiver Data Inverted.        | CML-O       | 3             | Output from Host |       |
| 34  | GND       | Module Ground.                 |             | 1             |                  |       |
| 35  | Rx4+      | Receiver Data Non-Inverted.    | CML-O       | 3             | Output from Host |       |

|    |          |                                |             |   |                  |   |
|----|----------|--------------------------------|-------------|---|------------------|---|
| 36 | Rx4-     | Receiver Data Inverted.        | CML-O       | 3 | Output from Host |   |
| 37 | GND      | Module Ground.                 |             | 1 |                  |   |
| 38 | Rx6+     | Receiver Data Non-Inverted.    | CML-O       | 3 | Output from Host |   |
| 39 | Rx6-     | Receiver Data Inverted.        | CML-O       | 3 | Output from Host |   |
| 40 | GND      | Module Ground.                 |             | 1 |                  |   |
| 41 | Rx8+     | Receiver Data Non-Inverted.    | CML-O       | 3 | Output from Host |   |
| 42 | Rx8-     | Receiver Data Inverted.        | CML-O       | 3 | Output from Host |   |
| 43 | GND      | Module Ground.                 |             | 1 |                  |   |
| 44 | INT/RSTn | Module Interrupt/Module Reset. | Multi-Level | 3 | Bi-Directional   | 2 |
| 45 | Vcc      | +3.3V Power.                   |             | 2 | Power from Host  |   |
| 46 | Vcc      | +3.3V Power.                   |             | 2 | Power from Host  |   |
| 47 | SDA      | 2-Wire Serial Interface Data.  | LVCMOS-I/O  | 3 | Bi-Directional   | 1 |
| 48 | GND      | Module Ground.                 |             | 1 |                  |   |
| 49 | Tx7-     | Transmitter Data Inverted.     | CML-I       | 3 | Input from Host  |   |
| 50 | Tx7+     | Transmitter Data Non-Inverted. | CML-I       | 3 | Input from Host  |   |
| 51 | GND      | Module Ground.                 |             | 1 |                  |   |
| 52 | Tx5-     | Transmitter Data Inverted.     | CML-I       | 3 | Input from Host  |   |
| 53 | Tx5+     | Transmitter Data Non-Inverted. | CML-I       | 3 | Input from Host  |   |
| 54 | GND      | Module Ground.                 |             | 1 |                  |   |
| 55 | Tx3-     | Transmitter Data Inverted.     | CML-I       | 3 | Input from Host  |   |
| 56 | Tx3+     | Transmitter Data Non-Inverted. | CML-I       | 3 | Input from Host  |   |
| 57 | GND      | Module Ground.                 |             | 1 |                  |   |
| 58 | Tx1-     | Transmitter Data Inverted.     | CML-I       | 3 | Input from Host  |   |
| 59 | Tx1+     | Transmitter Data Non-Inverted. | CML-I       | 3 | Input from Host  |   |
| 60 | GND      | Module Ground.                 |             | 1 |                  |   |

**Notes:**

1. Open-drain with pull-up resistor on the host.
2. See below for the required circuit.

Electrical Pin-Out Details



Block Diagram



Mechanical Specifications



Bending Radius

| Wire Gauge | OD (Ref.) | Bend Radius "R" | Min. Bend Radius "L" |
|------------|-----------|-----------------|----------------------|
| 30AWG      | 9.5mm     | 19mm            | 65mm                 |

# About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.

