



## CFP4-100GB-ER4-SKY

MSA Compliant 100GBase-ER4 CFP4 Transceiver (SMF, 1310nm, 40km, LC, DOM)

### Product Description

This MSA compliant CFP4 transceiver provides 100GBase-ER4 throughput up to 40km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

### Features:

- CFP MSA 1.1 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



### Applications:

- 100GBase Ethernet
- Access and Enterprise

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*For your product safety, please read the following information carefully before any manipulation of the transceiver:*



#### **ESD**

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



#### **LASER SAFETY**

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

*The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.*

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### Absolute Maximum Ratings

| Parameter                   | Symbol          | Min. | Max. | Unit |
|-----------------------------|-----------------|------|------|------|
| Storage Temperature         | T <sub>s</sub>  | -40  | +85  | °C   |
| Supply Voltage              | V <sub>cc</sub> | -0.5 | 3.6  | V    |
| Operating Relative Humidity | RH              | 5    | 95   | %    |

### Note:

1. Exceeding any one of these values may destroy the device immediately.

### Recommended Operating Conditions

| Parameter                                  | Symbol          |                | Min. | Typ.                | Max. | Unit |
|--------------------------------------------|-----------------|----------------|------|---------------------|------|------|
| Operating Case Temperature                 | T <sub>C</sub>  |                | 0    |                     | 70   | °C   |
| Power Supply Voltage                       | V <sub>cc</sub> |                | 3.2  | 3.3                 | 3.4  | V    |
| Power Supply Noise                         | DC-1MHz         |                |      | 2                   |      | %    |
|                                            | 1-10MHz         |                |      | 3                   |      |      |
| Power Consumption                          | P               | MAX            |      |                     | 6    | W    |
|                                            |                 | Low Power Mode |      |                     | 1    |      |
| Time of Power-On sequence & Reset Sequence |                 |                |      | TBD                 |      | sec  |
| Modulation Format                          |                 |                |      | NRZ, Mark Ratio 50% |      |      |

## Electrical Characteristics

| Parameter                       | Symbol           | Min. | Typ. | Max. | Unit | Notes                            |
|---------------------------------|------------------|------|------|------|------|----------------------------------|
| Transmitter                     |                  |      |      |      |      |                                  |
| Input Amplitude (Differential)  | V <sub>in</sub>  | 150  |      | 1000 | mVpp | AC coupled inputs, 1             |
| Input Impedance (Differential)  | Z <sub>in</sub>  | 85   | 100  | 115  | ohms | R <sub>in</sub> > 100 kohms @ DC |
| Receiver                        |                  |      |      |      |      |                                  |
| Output Amplitude (Differential) | V <sub>out</sub> | 360  |      | 900  | mVpp | AC coupled Outputs, 1            |
| Output Impedance (Differential) | Z <sub>out</sub> | 85   | 100  | 115  | ohms |                                  |

### Notes:

1. High speed I/O, internally AC coupled.

## 1.2V MDIO Interface Specifications

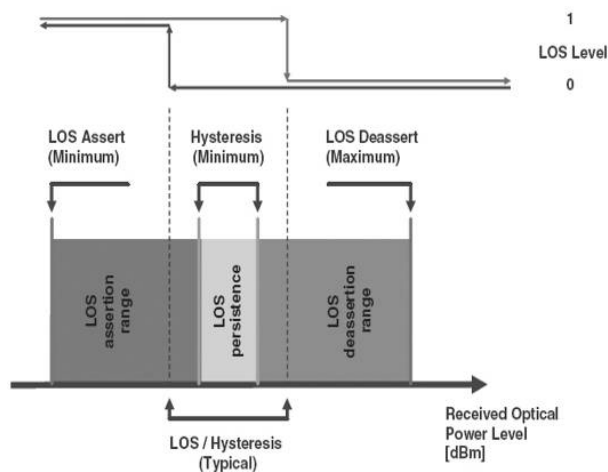
| Parameter                          | Symbol                   | Min. | Typ. | Max.  | Unit | Notes |
|------------------------------------|--------------------------|------|------|-------|------|-------|
| Input Voltage                      | V <sub>IH</sub>          | 0.84 |      | 1.5   | V    |       |
|                                    | V <sub>IL</sub>          | -0.3 |      | 0.36  | V    |       |
| Input Leak current                 | I <sub>IN</sub>          | -100 |      | 100   | uA   |       |
| Output Voltage                     | V <sub>OH</sub>          | 1.0  |      | 1.5   | V    |       |
|                                    | V <sub>OL</sub>          | -0.3 |      | 0.2   | V    |       |
| Input Capacitance                  | C <sub>I</sub>           |      |      | 10    | pF   |       |
| Input MDC Clock                    | f <sub>MDC</sub>         | 0.1  |      | 4     | MHz  |       |
| MDC Clock Period                   | T <sub>MDC</sub>         | 250  |      | 10000 | ns   |       |
| MDIO Hold Time                     | T <sub>hold</sub>        | 10   |      |       | ns   |       |
| MDIO Setup Time                    | T <sub>Setup</sub>       | 10   |      |       | ns   |       |
| Clock to output delay from the MMD | T <sub>dely</sub>        | 0    |      | 300   | ns   |       |
| GLB_ALM                            | T <sub>glb_alm_ass</sub> |      |      | 150   | ms   |       |
|                                    | T <sub>glb_alm_dea</sub> |      |      | 150   | ms   |       |
| MDC High time                      | T <sub>high</sub>        |      |      | 160   | ns   |       |
| MDC Low time                       | T <sub>low</sub>         |      |      | 160   | ns   |       |

## Optical Characteristics

| Parameter                                                | Symbol            | Min.                               | Typ.    | Max.    | Unit | Notes |
|----------------------------------------------------------|-------------------|------------------------------------|---------|---------|------|-------|
| Transmitter                                              |                   |                                    |         |         |      |       |
| Signaling Speed per Lane                                 | BR <sub>AVE</sub> |                                    | 25.78   |         | Gbps |       |
| Signaling Speed per Lane OTU4                            | BR <sub>AVE</sub> |                                    | 27.95   |         | Gbps |       |
| Data Rate Variation                                      |                   | -100                               |         | +100    | ppm  |       |
| Lane_0 Center Wavelength                                 | λC0               | 1294.53                            | 1295.56 | 1296.59 | nm   |       |
| Lane_1 Center Wavelength                                 | λC1               | 1299.02                            | 1300.05 | 1301.09 | nm   |       |
| Lane_2 Center Wavelength                                 | λC2               | 1303.54                            | 1304.58 | 1305.63 | nm   |       |
| Lane_3 Center Wavelength                                 | λC3               | 1308.09                            | 1309.14 | 1310.19 | nm   |       |
| Total Average Output Power                               | Po                |                                    |         | 12.5    | dBm  | 1     |
| Average Launch Power per Lane                            | P <sub>each</sub> | -2.5                               |         | 6.5     | dBm  |       |
| Optical Modulation Amplitude per Lane                    |                   | 0.5                                |         | 6.5     | dBm  |       |
| Average launch power of OFF transmitter per lane         |                   |                                    |         | -30     | dBm  |       |
| Optical Return Loss Tolerance                            |                   |                                    |         | 20      | dB   |       |
| Extinction Ratio                                         | ER                | 4.5                                |         |         | dB   | 4     |
| Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} |                   | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} |         |         |      | 4     |
| TX Disable Assert Time                                   | t <sub>off</sub>  |                                    |         | 100     | us   |       |
| Receiver                                                 |                   |                                    |         |         |      |       |
| Signaling Speed per Lane                                 | BR <sub>AVE</sub> |                                    | 25.78   |         | Gbps |       |
| Signaling Speed per Lane OTU4                            | BR <sub>AVE</sub> |                                    | 27.95   |         | Gbps |       |
| Data Rate Variation                                      |                   | -100                               |         | +100    | ppm  |       |
| Damage threshold                                         | R <sub>dam</sub>  | -2.5                               |         |         | dBm  |       |
| Lane_0 Center Wavelength                                 | λC0               | 1294.53                            | 1295.56 | 1296.59 | nm   |       |
| Lane_1 Center Wavelength                                 | λC1               | 1299.02                            | 1300.05 | 1301.09 | nm   |       |
| Lane_2 Center Wavelength                                 | λC2               | 1303.54                            | 1304.58 | 1305.63 | nm   |       |
| Lane_3 Center Wavelength                                 | λC3               | 1308.09                            | 1309.14 | 1310.19 | nm   |       |
| Average Receive Power                                    | R <sub>pow</sub>  | -20.5                              |         | TBD     | dBm  |       |
| Receive Sensitivity in OMA per Lane                      | P <sub>min</sub>  |                                    |         | -18.5   | dBm  | 5     |
| LOS Assert                                               | LOSA              | -30                                |         |         | dBm  |       |
| LOS De-Assert                                            | LOSD              |                                    |         | -20     | dBm  |       |
| LOS Hysteresis                                           |                   | 0.5                                |         |         | dB   | 3     |

### Notes:

1. Output is coupled into a 9/125µm single-mode fiber.
2. High speed I/O, internally AC coupled.
3. LOS Hysteresis
4. Filtered, measured with a PRBS 231-1 test pattern @25.78Gbps
5. Receiver sensitivity (OMA), each lane (max) is informative, BER =  $5 \times 10^{-5}$



### MDIO Registers for MCLK

| MDIO Hex Addr | Access Type | Bit       | Register Name   | Value and Description                                                                                                                         | Notes |
|---------------|-------------|-----------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A011h         | R/W         | 7:5       | TX MCLK Control | 000b: Disabled (Initial Value)<br>010b: 1/8 of network lane                                                                                   |       |
| A012h         | R/W         | 7:5       | RX MCLK Control | 000b: Disabled (Initial Value)<br>010b: 1/8 of network lane                                                                                   |       |
| A015h         | R/W         | 13:1<br>2 | MCLK Selection  | Selects the source of the MCLK for CFP4 modules.<br>00b: MCLK Off (Initial Value).<br>01b: MCLK = TX_MCLK<br>10b: Reserved.<br>11b: Reserved. |       |

### MDIO Registers for Host Lane Control Controls Selection

| MDIO Hex Addr | Access Type | Bit  | Register Name                    | Value and Description                                                                                                                      | Notes |
|---------------|-------------|------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A440~A443h    | R/W         | 15   | Signal equalization mode control | 0: Automatic (Initial Value) 1: Manual                                                                                                     |       |
|               | R/W         | 12~9 | Signal Equalization Gain         | 00h: No EQ (Initial Value).<br>Write 9~0 to set 9 ~ 0 Db of gain in manual mode.                                                           |       |
|               | R/W         | 3~0  | Rx Signal Pre/De-emphasis        | 0000b: 0dB (Initial Value).<br>4-bit unsigned number N represents the pre/de-emphasis applied.<br>Pre/De-emphasis = 0.5 dB * N, N = 0, 15. |       |

### MDIO Registers for Host Lane RX Squelch Mode Selection

| MDIO Hex Addr | Access Type | Bit  | Register Name                             | Value and Description                                                                                                                                                                                    | Notes |
|---------------|-------------|------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A014h         | R/W         | 9    | Automatic Host Lane Output Squelch on LOS | 0: Host Lane shall not squelch Rx RF output on RX_LOS. Host controls squelch using A040h (Initial Value).<br>1: Host Lane shall squelch Rx RF output on RX_LOS (sync with A210h~A21Fh.4) per lane based. |       |
| A040h         | R/W         | 15~0 | Host Lane Output Squelch Control          | Bits 15~0 squelches host lane 15~0 Rx RF output respectively.<br>0: No squelch (Initial Value).<br>1: Squelch.                                                                                           |       |

### MDIO Registers for Network Lane Squelch & Disable Selection

| MDIO Hex Addr | Access Type | Bit  | Register Name                             | Value and Description                                                                                                                                                                                              | Notes |
|---------------|-------------|------|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A011h         | R/W         | 15   | Automatic Network Lane TX Squelch Mode    | 0: Network Lane shall squelch TX Average power on TX_LOL (sync with A210h~A21Fh.6) per lane base (Initial Value).<br>1: Network Lane shall squelch TX OMA power on TX_LOL (sync with A210h~A21Fh.6) per lane base. |       |
|               | R/W         | 4    | Automatic Network Lane TX Squelch Control | 0: Network lane automatic control on TX_LOL is off. Host controls each lane TX squelch using A041h (Initial Value).<br>1: Network lane automatic control on TX_LOL is on per lane base.                            |       |
| A013h         | R/W         | 15~0 | Lane 15~0 Disable                         | Bits 15~0 disable network lane 15~0 Tx Average power output respectively.<br>0: Normal (Initial Value).<br>1: Disable.                                                                                             |       |
| A041h         | R/W         | 15~0 | Network Lane n TX Squelch                 | Bits 15~0 squelches network lane 15~0 Tx OMA power output respectively.<br>0: No squelch (Initial Value).<br>1: Squelch.                                                                                           |       |

#### MDIO Registers for TX/Rx Reset

| MDIO Hex Addr | Access Type | Bit | Register Name | Value and Description                             | Notes |
|---------------|-------------|-----|---------------|---------------------------------------------------|-------|
| A011h         | R/W         | 8   | TX Reset      | 0: Normal operation (Initial Value),<br>1: Reset. | 1     |
| A012h         | R/W         | 8   | RX Reset      | 0: Normal operation (Initial Value),<br>1: Reset. | 1     |

#### Notes:

1. Set these registers to 1 will keep the correspond CDR in reset state. While these bits are cleared, the correspond CDR will be re-initialized.

#### MDIO Registers for PRG\_CNTL1/Tx\_DIS

| MDIO Hex Addr | Access Type | Bit | Register Name        | Value and Description                                                                                                                                                                                                                                      | Notes |
|---------------|-------------|-----|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A007h         | R/W         | 7~0 | Function Select Code | 0: Assert/De-Assert of PRG_CNTL1 has no effect.<br>0x01: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1.<br>When so assigned this pin uses the active low logic, that is, 0 =Assert (Reset).<br>2~9: MSA reserved.<br>0x0A: TX_DIS (Initial Value). | 1     |

#### Notes:

1. CFP4 module multiplexes PRG\_CNTL1 with TX\_DIS functions. Host shall use this register to assign TX\_DIS function to PRG\_CNTL1, if and only if module is in Low\_Power State. When A007h is set to 0x01 in low power state, then the TRXIC\_RSTn function is enabled and the hardware TX\_DIS is assigned to be de-asserted.

#### MDIO Registers for PRG\_ALARM1

| MDIO Hex Addr | Access Type | Bit | Register Name     | Value and Description                                                                                                                                                                                                                                                                                                               | Notes |
|---------------|-------------|-----|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A00Ah         | R/W         | 7~0 | Alarm Source Code | 0: Not active, always de-asserted,<br>1: HIPWR_ON, MSA default setting,<br>2: Ready State,<br>3: Fault State,<br>4: RX_ALARM = RX_LOS + RX_NETWORK_LOL,<br>5: TX_ALARM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL,<br>6: RX_NETWORK_LOL,<br>7: TX_LOSF,<br>8: TX_HOST_LOL,<br>9: OOA,<br>10: RX_LOS (Initial Value).<br>11~255: Reserved. |       |

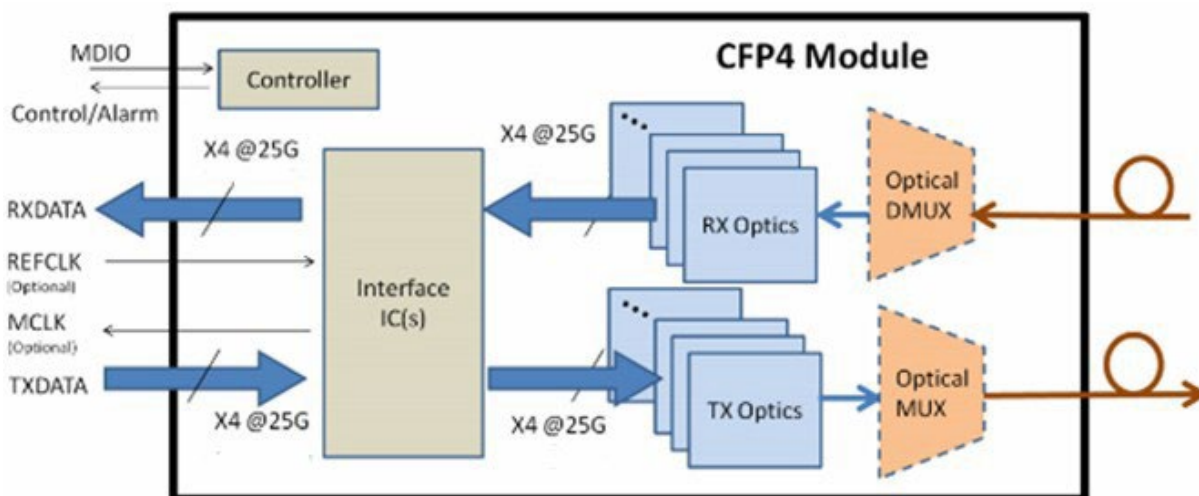
### MDIO Registers for RX Power Monitor Alarm/Warning Threshold

| MDIO Hex Addr | Access Type | Bit  | Register Name                                                | Value and Description                                                                                                                                                                                                                                                     | Notes |
|---------------|-------------|------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| A015h         | R/W         | 9    | RX Power Monitor Alarm/Warning Threshold Select              | 0: MSA default registers 80C0h~80C7h (Initial Value),<br>1: Host Configured Receive Optical Power Threshold registers A03Ch~A03Fh.                                                                                                                                        | 1     |
| A03Ch         | R/W         | 15~0 | Host Configured Receive Optical Power High Alarm Threshold   | Valid if the value is between “Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold” (80E8h) and “Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold” (80F0h). Value beyond the threshold shall generate no effect. |       |
| A03Dh         | R/W         | 15~0 | Host Configured Receive Optical Power High Warning Threshold | Valid if the value is between “Host Configured Optical Power High Warning Permissible Minimum Threshold” (0x80EA) and “Host Configured Optical Power High Warning Permissible Maximum Threshold” (80F2h). Value beyond the threshold shall generate no effect.            |       |
| A03Eh         | R/W         | 15~0 | Host Configured Receive Optical Power Low Warning Threshold  | Valid if the value is between “Host Configured Optical Power Low Warning Permissible Minimum Threshold” (80Ech) and “Host Configured Optical Power Low Warning Permissible Maximum Threshold” (80F4h). Value beyond the threshold shall generate no effect.               |       |
| A03Fh         | R/W         | 15~0 | Host Configured Receive Optical Power Low Alarm Threshold    | Valid if the value is between “Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold” (80Eeh) and “Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold” (80F6h). Value beyond the threshold shall generate no effect.   |       |

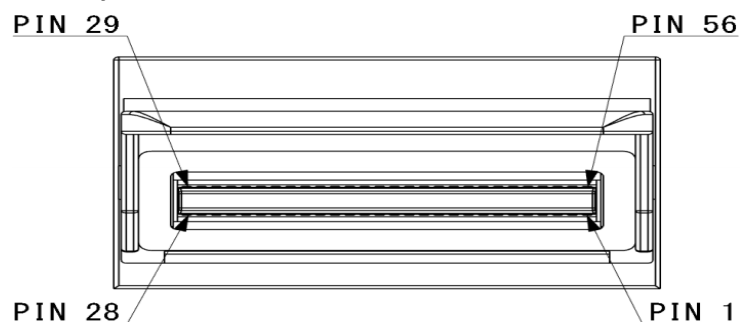
#### Notes:

1. Set these registers to 1 will keep the correspond CDR in reset state. While these bits are cleared, the correspond CDR will be re-initialized.

## Functional Description of Transceiver



## CFP4 Transceiver Electrical Pad Layout



## Pin Descriptions

### Part A: Bottom Row Pin Function Definition

| Pin | Name     | Function                   | Description                                                      |
|-----|----------|----------------------------|------------------------------------------------------------------|
| 1   | 3.3V_GND | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground |
| 2   | 3.3V_GND | Ground                     |                                                                  |
| 3   | 3.3V     | 3.3V Module Supply Voltage | 3.3V ± 5%                                                        |
| 4   | 3.3V     | 3.3V Module Supply Voltage | 3.3V ± 5%                                                        |
| 5   | 3.3V     | 3.3V Module Supply Voltage | 3.3V ± 5%                                                        |
| 6   | 3.3V     | 3.3V Module Supply Voltage | 3.3V ± 5%                                                        |
| 7   | 3.3V_GND | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground |
| 8   | 3.3V_GND | Ground                     | 3.3V Module Supply Ground, Internally connected to Signal Ground |
| 9   | VND_IO_A | I/O                        | Module Vendor I/O A. NC                                          |
| 10  | VND_IO_B | I/O                        | Module Vendor I/O B, NC                                          |

|    |                       |                  |                                                                                |
|----|-----------------------|------------------|--------------------------------------------------------------------------------|
| 11 | TX_DIS<br>(PRG_CNTL1) | I                | "1" or NC = transmitter disabled,<br>"0" = transmitter enabled                 |
| 12 | RX_LOS<br>(PRG_ALRM1) | O                | "1" = loss of signal (low optical signal), "0" = normal condition              |
| 13 | GLB_ALRMn             | O                | "0" = alarm condition in any MDIO Alarm register,<br>"1" = no alarm condition, |
| 14 | MOD_LOPWR             | I                | "1" or NC = module in low power (safe) mode,<br>"0" = power-on enabled         |
| 15 | MOD_ABS               | O                | "1" or NC = module absent,<br>"0" = module present                             |
| 16 | MOD_RSTn              | I                | "0" = resets the module,<br>"1" or NC = module enabled                         |
| 17 | MDC                   | 1.2V COMS<br>I   | Management Data Clock                                                          |
| 18 | MDIO                  | 1.2V COMS<br>I/O | Management Data I/O bi-directional data                                        |
| 19 | PRTADR0               | 1.2V COMS<br>I   | MDIO Physical Port address bit 0                                               |
| 20 | PRTADR1               | 1.2V COMS<br>I   | MDIO Physical Port address bit 1                                               |
| 21 | PRTADR2               | 1.2V COMS<br>I   | MDIO Physical Port address bit 2                                               |
| 22 | VND_IO_C              | I/O              | Module Vendor I/O C. NC                                                        |
| 23 | VND_IO_D              | I/O              | Module Vendor I/O D. NC                                                        |
| 24 | VND_IO_E              | I/O              | Module Vendor I/O E. NC                                                        |
| 25 | GND                   | Ground           | Signal Ground                                                                  |
| 26 | (MCLKn)               | CML<br>O         | For optical waveform testing                                                   |
| 27 | (MCLKp)               | CML<br>O         | For optical waveform testing                                                   |
| 28 | GND                   | Ground           | Signal Ground                                                                  |

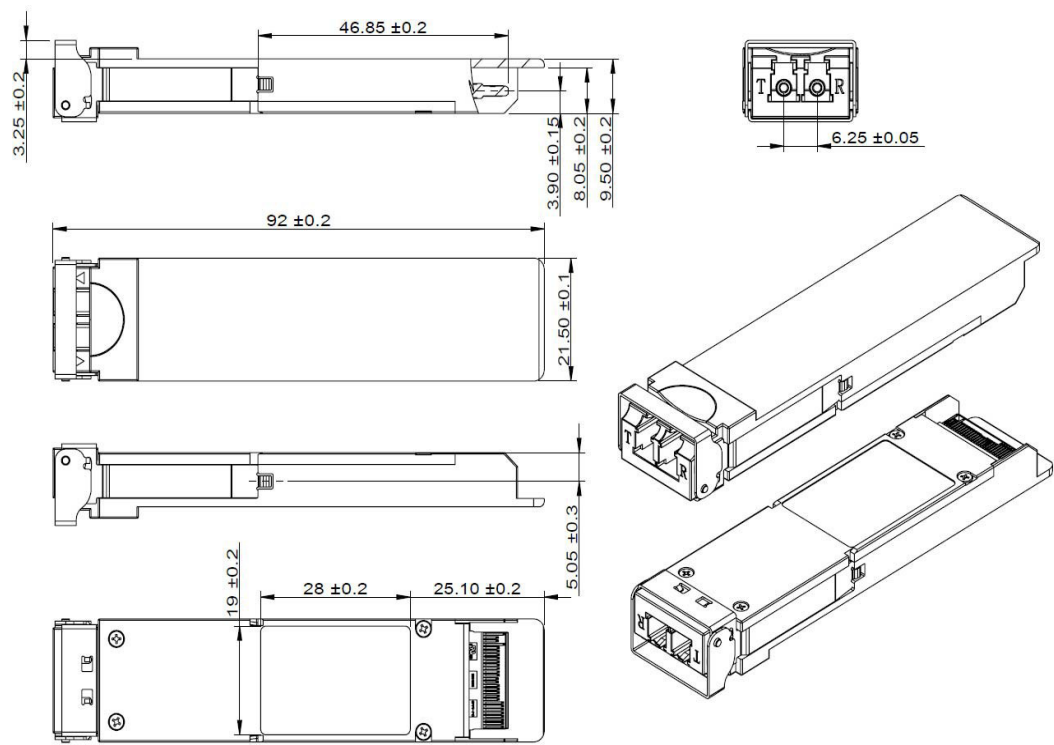
#### Part B: Top Row Pin Function Definition

| Pin | Name | Function             | Description   |
|-----|------|----------------------|---------------|
| 56  | GND  | Ground               | Signal Ground |
| 55  | TX3n | Lane 3 Tx Input<br>I | CML Input     |
| 54  | TX3p | Lane 3 Tx Input<br>I | CML Input     |
| 53  | GND  | Ground               | Signal Ground |
| 52  | TX2n | Lane 2 Tx Input<br>I | CML Input     |
| 51  | TX2p | Lane 2 Tx Input<br>I | CML Input     |
| 50  | GND  | Ground               | Signal Ground |
| 49  | TX1n | Lane 1 Tx Input<br>I | CML Input     |

|    |           |                       |                       |
|----|-----------|-----------------------|-----------------------|
| 48 | TX1p      | Lane 1 Tx Input<br>I  | CML Input             |
| 47 | GND       | Ground                | Signal Ground         |
| 46 | TX0n      | Lane 0 Tx Input<br>I  | CML Input             |
| 45 | TX0p      | Lane 0 Tx Input<br>I  | CML Input             |
| 44 | GND       | Ground                | Signal Ground         |
| 43 | (REFCLKn) | Reference Clock<br>I  | Reference Clock Input |
| 42 | (REFCLKp) | Reference Clock<br>I  | Reference Clock Input |
| 41 | GND       | Ground                | Signal Ground         |
| 40 | RX3n      | Lane 3 Rx Output<br>O | CML Output            |
| 39 | RX3p      | Lane 3 Rx Output<br>O | CML Output            |
| 38 | GND       | Ground                | Signal Ground         |
| 37 | RX2n      | Lane 2 Rx Output<br>O | CML Output            |
| 36 | RX2p      | Lane 2 Rx Output<br>O | CML Output            |
| 35 | GND       | Ground                | Signal Ground         |
| 34 | RX1n      | Lane 1 Rx Output<br>O | CML Output            |
| 33 | RX1p      | Lane 1 Rx Output<br>O | CML Output            |
| 32 | GND       | Ground                | Signal Ground         |
| 31 | RX0n      | Lane 0 Rx Output<br>O | CML Output            |
| 30 | RX0p      | Lane 0 Rx Output<br>O | CML Output            |
| 29 | GND       | Ground                | Signal Ground         |

Mechanical Specifications

| Parameter | Symbol | Max. | Unit | Spec                                                  |
|-----------|--------|------|------|-------------------------------------------------------|
| Weight    |        | 90   | g    |                                                       |
| Flatness  |        | 0.12 | mm   | CFP MSA CFP4 HW spec<br>Rev.0.1_5.3.1=0.12mm(class=4) |
| Roughness | Ra     | 1.6  | μm   | CFP MSA CFP4 HW spec<br>Rev.0.1_5.3.1=0.16mm(class=4) |



# About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.

