



## C2Q00000C00D000

MSA 100GBase-Converter CFP2 Transceiver (CFP2 to QSFP28 Converter)

### Product Description

This MSA Compliant QSFP28 to QSFP28 converter provides conversion from CFP2 to QSFP28 form factors. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

### Features:

- Compatible with CFP2 MSA Specification
- Single 3.3V Power Supply and Power Dissipation < 1.8W
- Compatible with QSFP28 MSA Specification
- Hot Pluggable 104-Pin Connector
- 4x 25G CFP2 Electrical Plug Interface Provided
- Case Temperature Range: 0 to 70
- 4x 25G QSFP28 Electrical Socket Interface Provided
- RoHS compliant and Lead Free
- Management and Control via MDIO 2-Wire Interface



### Applications:

- 100GBase Ethernet
- Access and Enterprise

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*For your product safety, please read the following information carefully before any manipulation of the transceiver:*



#### ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



#### LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

*The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.*

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## Absolute Maximum Ratings

| Parameter                  | Symbol | Min. | Typ.    | Max.  | Unit | Notes |
|----------------------------|--------|------|---------|-------|------|-------|
| Storage Temperature        | Tstg   | -40  |         | 85    | °C   |       |
| Operating Case Temperature | Tc     | 0    |         | 70    | °C   |       |
| Power Supply Current       | Icc    |      |         | 550   | mA   |       |
| Aggregate Bit Rate         | BRave  |      | 103.125 | 111.8 | Gbps |       |
| Lane Bit Rate              | BRlane |      | 25.78   | 27.95 | Gbps |       |

## Electrical Characteristics

| Parameter                     |         | Symbol | Min.  | Typ. | Max.    | Unit  | Notes |
|-------------------------------|---------|--------|-------|------|---------|-------|-------|
| Power Supply Voltage          |         | Vcc    | 3.135 | 3.3  | 3.465   | V     |       |
| Transmitter                   |         |        |       |      |         |       |       |
| Differential Input Amplitude  |         | VIN    | 150   |      | 1000    | mVp-p | 1     |
| Differential Input Impedance  |         | ZIN    | 85    | 100  | 115     | Ω     | 2     |
| Tx_Disable                    | Disable | VIH    | 2     |      | Vcc+0.3 | V     |       |
|                               | Enable  | VIL    | 0     |      | 0.8     | V     |       |
| Receiver                      |         |        |       |      |         |       |       |
| Differential Output Amplitude |         | VOUT   | 340   |      | 400     | mVp-p | 3     |
| Differential Output Impedance |         | ZOUT   | 85    | 100  | 115     | Ω     |       |
| Output Rise/Fall Time         |         | Tr/Tf  | 24    |      |         | ps    | 4     |
| Rx_LOS                        | LOS     | VOH    | 2.4   |      | Vcc+0.3 | V     |       |
|                               | Normal  | VOL    | 0     |      | 0.8     | V     |       |

### Notes:

1. AC coupled inputs.
2. RIN > 100kΩ @ DC.
3. AC coupled outputs.
4. 20-80%.

## 1.2V MDIO Interface Specifications

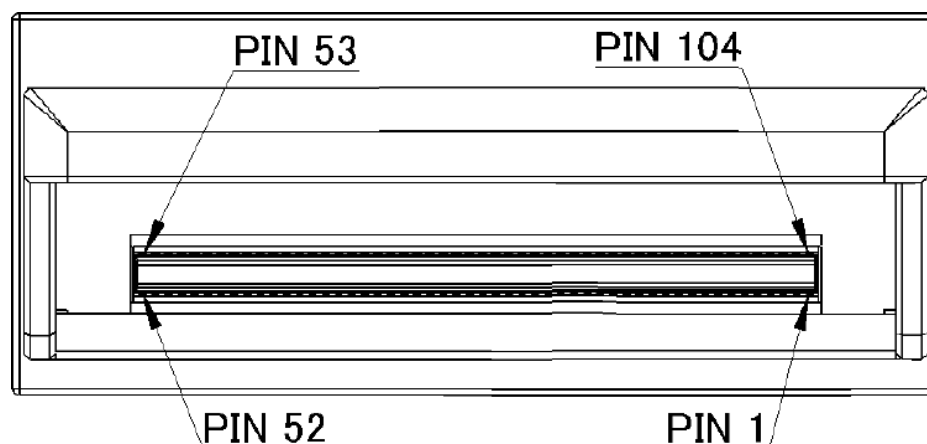
| Parameter          | Symbol       | Min. | Typ. | Max.  | Unit | Notes |
|--------------------|--------------|------|------|-------|------|-------|
| Input Voltage      | VIH          | 0.84 |      | 1.5   | V    |       |
|                    | VIL          | -0.3 |      | 0.36  | V    |       |
| Input Leak Current | IIN          | -100 |      | 100   | uA   |       |
| Output Voltage     | VOH          | 1.0  |      | 1.5   | V    |       |
|                    | VOL          | -0.3 |      | 0.2   | V    |       |
| Input Capacitance  | Ci           |      |      | 10    | pF   |       |
| Input MDC Clock    | fMDC         | 0.1  |      | 4     | MHz  |       |
| MDC Clock Period   | tMDC         | 250  |      | 10000 | ns   |       |
| MDIO Hold Time     | Thold        | 10   |      |       | ns   |       |
| MDIO Setup Time    | Tsetup       | 10   |      |       | ns   |       |
| GLB_ALM            | Tglb_alm_ass |      |      | 150   | ms   |       |
|                    | Tglb_alm_dea |      |      | 150   | ms   |       |

## CFP2 Pin Function Definitions

| Bottom |            | Top |      |
|--------|------------|-----|------|
| 1      | GND        | 53  | GND  |
| 2      | (TX_MCK_N) | 54  | N.C. |
| 3      | (TX_MCK_P) | 55  | N.C. |
| 4      | GND        | 56  | GND  |
| 5      | N.C.       | 57  | Rx0+ |
| 6      | N.C.       | 58  | Rx0- |
| 7      | 3.3V_GND   | 59  | GND  |
| 8      | 3.3V_GND   | 60  | Rx1+ |
| 9      | 3.3V       | 61  | Rx1- |
| 10     | 3.3V       | 62  | GND  |
| 11     | 3.3V       | 63  | N.C. |
| 12     | 3.3V       | 64  | N.C. |
| 13     | 3.3V_GND   | 65  | GND  |
| 14     | 3.3V_GND   | 66  | N.C. |
| 15     | VND_IO_A   | 67  | N.C. |
| 16     | VND_IO_B   | 68  | GND  |
| 17     | PRG_CNTL1  | 69  | Rx2+ |
| 18     | PRG_CNTL2  | 70  | Rx2- |
| 19     | PRG_CNTL3  | 71  | GND  |
| 20     | PRG_ALARM1 | 72  | Rx3+ |
| 21     | PRG_ALARM2 | 73  | Rx3- |
| 22     | PRG_ALARM3 | 74  | GND  |
| 23     | GND        | 75  | N.C. |

|    |            |     |           |
|----|------------|-----|-----------|
| 24 | Tx_Disable | 76  | N.C.      |
| 25 | Rx_LOS     | 77  | GND       |
| 26 | MOD_LOPWR  | 78  | (REFCLKp) |
| 27 | MOD_ABS    | 79  | (REFCLKp) |
| 28 | MOD_RSTn   | 80  | GND       |
| 29 | GLB_ALRMn  | 81  | N.C.      |
| 30 | GND        | 82  | N.C.      |
| 31 | MDC        | 83  | GND       |
| 32 | MDIO       | 84  | Tx0+      |
| 33 | PRTADR0    | 85  | Tx0-      |
| 34 | PRTADR1    | 86  | GND       |
| 35 | PRTADR2    | 87  | Tx1+      |
| 36 | VND_IO_C   | 88  | Tx1-      |
| 37 | VND_IO_D   | 89  | GND       |
| 38 | VND_IO_E   | 90  | N.C       |
| 39 | 3.3V_GND   | 91  | N.C.      |
| 40 | 3.3V_GND   | 92  | GND       |
| 41 | 3.3V       | 93  | N.C       |
| 42 | 3.3V       | 94  | N.C       |
| 43 | 3.3V       | 95  | GND       |
| 44 | 3.3V       | 96  | Tx2+      |
| 45 | 3.3V_GND   | 97  | Tx2-      |
| 46 | 3.3V_GND   | 98  | GND       |
| 47 | N.C.       | 99  | Tx3+      |
| 48 | N.C.       | 100 | Tx3-      |
| 49 | GND        | 101 | GND       |
| 50 | (RX_MCK_N) | 102 | N.C       |
| 51 | (RX_MCK_P) | 103 | N.C.      |
| 52 | GND        | 104 | GND       |

## CFP2 Electrical Pad Layout



## Bottom Row Pin Descriptions

| Pin | Symbol     | Function      | Notes |
|-----|------------|---------------|-------|
| 1   | GND        |               |       |
| 2   | (TX_MCK_N) | O CML         | 1     |
| 3   | (TX_MCK_P) | O CML         | 1     |
| 4   | GND        |               |       |
| 5   | N.C.       |               |       |
| 6   | N.C.       |               |       |
| 7   | 3.3V_GND   |               |       |
| 8   | 3.3V_GND   |               |       |
| 9   | 3.3V       |               | 2     |
| 10  | 3.3V       |               | 2     |
| 11  | 3.3V       |               | 2     |
| 12  | 3.3V       |               | 2     |
| 13  | 3.3V_GND   |               |       |
| 14  | 3.3V_GND   |               |       |
| 15  | VND_IO_A   |               | 3     |
| 16  | VND_IO_B   |               | 4     |
| 17  | PRG_CNTL1  |               | 5     |
| 18  | PRG_CNTL2  |               | 6     |
| 19  | PRG_CNTL3  |               | 7     |
| 20  | PRG_ALARM1 |               | 8     |
| 21  | PRG_ALARM2 |               | 9     |
| 22  | PRG_ALARM3 |               | 10    |
| 23  | GND        |               |       |
| 24  | Tx_Disable | I LVCMOS      | 11    |
| 25  | Rx_LOS     | O LVCMOS      | 12    |
| 26  | MOD_LOPWR  | I LVCMOS      | 13    |
| 27  | MOD_ABS    | O GND         | 14    |
| 28  | MOD_RSTn   | I LVCMOS      | 15    |
| 29  | GLB_ALARMn | O LVCMOS      | 16    |
| 30  | GND        |               |       |
| 31  | MDC        | I 1.2V CMOS   | 17    |
| 32  | MDIO       | I/O 1.2V CMOS | 18    |
| 33  | PRTADR0    | I 1.2V CMOS   | 19    |
| 34  | PRTADR1    | I 1.2V CMOS   | 20    |
| 35  | PRTADR2    | I 1.2V CMOS   | 21    |

|    |            |       |    |
|----|------------|-------|----|
| 36 | VND_IO_C   | I/O   | 22 |
| 37 | VND_IO_D   | I/O   | 23 |
| 38 | VND_IO_E   | I/O   | 24 |
| 39 | 3.3V_GND   |       |    |
| 40 | 3.3V_GND   |       |    |
| 41 | 3.3V       |       | 2  |
| 42 | 3.3V       |       | 2  |
| 43 | 3.3V       |       | 2  |
| 44 | 3.3V       |       | 2  |
| 45 | 3.3V_GND   |       |    |
| 46 | 3.3V_GND   |       |    |
| 47 | N.C.       |       | 25 |
| 48 | N.C.       |       | 25 |
| 49 | GND        |       |    |
| 50 | (RX_MCK_N) | O CML | 1  |
| 51 | (RX_MCK_P) | O CML | 1  |
| 52 | GND        |       |    |

#### Notes:

1. For optical waveform testing. Not for normal use.
2. 3.3V module supply voltage.
3. Module Vendor I/O A. Do not connect.
4. Module Vendor I/O B. Do not connect.
5. Programmable control 1 set over MDIO. MSA default: TRXIC\_RSTn/TX&RX ICs reset. "0" is reset, and "1" or "NC" means enabled/not used.
6. Programmable Control 2 set over MDIO. MSA default: Hardware Interlock LSB. "00" is  $\leq 3W$ , "01" is  $\leq 6W$ , "10" is  $\leq 9W$ , and "11" or NC is  $\leq 12W$  which is not used.
7. Programmable Control 3 set over MDIO. MSA default: Hardware Interlock MSB. "00" is  $\leq 3W$ , "01" is  $\leq 6W$ , "10" is  $\leq 9W$ , and "11" or NC is  $\leq 12W$  which is not used.
8. Programmable Alarm 1 set over MDIO. MSA default: HIPWR\_ON. "1" indicates that the module power-up is complete, and "0" indicates that the module is not high powered-up.
9. Programmable Alarm 2 set over MDIO. MSA default: MOD\_READY. "1" is ready, and "0" is not ready.
10. Programmable Alarm 3 set over MDIO. MSA default: MOD\_FAULT (fault detected). "1" is fault, and "0" is not fault.
11. Transmitter disables for all lanes. "1" or NC is transmitter disabled, and "0" is transmitter enabled.
12. Receiver loss of optical signal. "1" is low optical signal, and "0" is normal condition.
13. Module low-power mode. "1" or NC is module in low-power (safe) mode, and "0" is power-on enabled.
14. Module Absent. "1" or NC is module absent, and "0" is module present. Pull-up resistor on the host.
15. Module Reset. "0" resets the module, and "1" or NC is module enabled. Pull-down resistor in the module.
16. Global Alarm. "0" is the alarm condition in any MDIO alarm register, and "1" is no alarm condition. Open Drain. Pull-up resistor on the host.

17. Management Data Clock.
18. Management Data I/O Bi-Directional Data.
19. MDIO Physical Port Address Bit 0.
20. MDIO Physical Port Address Bit 1.
21. MDIO Physical Port Address Bit 2.
22. Module Vendor I/O C. Do not connect.
23. Module Vendor I/O D. Do not connect.
24. Module Vendor I/O E. Do not connect.
25. Not Connected.

#### Top Row Pin Descriptions

| Pin | Symbol    | Function           | Notes |
|-----|-----------|--------------------|-------|
| 53  | GND       |                    |       |
| 54  | N.C.      |                    |       |
| 55  | N.C.      |                    |       |
| 56  | GND       |                    |       |
| 57  | Rx0+      | Lane 0 Rx Output O | 1     |
| 58  | Rx0-      | Lane 0 Rx Output O | 1     |
| 59  | GND       |                    |       |
| 60  | Rx1+      |                    | 1     |
| 61  | Rx1-      |                    | 1     |
| 62  | GND       |                    |       |
| 63  | N.C.      |                    |       |
| 64  | N.C.      |                    |       |
| 65  | GND       |                    |       |
| 66  | N.C.      |                    |       |
| 67  | N.C.      |                    |       |
| 68  | GND       |                    |       |
| 69  | Rx2+      | Lane 2 Rx Output O | 1     |
| 70  | Rx2-      | Lane 2 Rx Output O | 1     |
| 71  | GND       |                    |       |
| 72  | Rx3+      | Lane 3 Rx Output O | 1     |
| 73  | Rx3-      | Lane 3 Rx Output O | 1     |
| 74  | GND       |                    |       |
| 75  | N.C.      |                    |       |
| 76  | N.C.      |                    |       |
| 77  | GND       |                    |       |
| 78  | (REFCLKn) | Reference Clock I  | 2     |

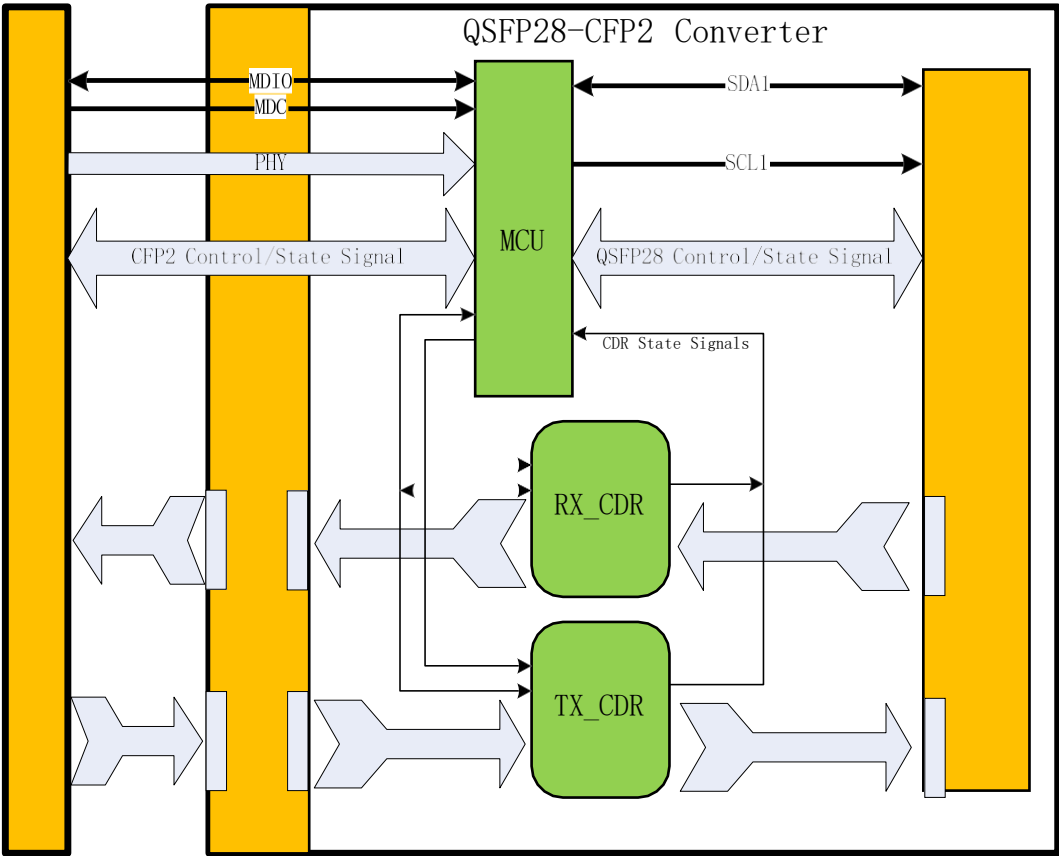
|     |           |                   |   |
|-----|-----------|-------------------|---|
| 79  | (REFCLKp) | Reference Clock I | 2 |
| 80  | GND       |                   |   |
| 81  | N.C.      |                   |   |
| 82  | N.C.      |                   |   |
| 83  | GND       |                   |   |
| 84  | Tx0+      | Lane 0 Tx Input I | 3 |
| 85  | Tx0-      | Lane 0 Tx Input I | 3 |
| 86  | GND       |                   |   |
| 87  | Tx1+      | Lane 1 Tx Input I | 3 |
| 88  | Tx1-      | Lane 1 Tx Input I | 3 |
| 89  | GND       |                   |   |
| 90  | N.C.      |                   |   |
| 91  | N.C.      |                   |   |
| 92  | GND       |                   |   |
| 93  | N.C.      |                   |   |
| 94  | N.C.      |                   |   |
| 95  | GND       |                   |   |
| 96  | Tx2+      | Lane 2 Tx Input I | 3 |
| 97  | Tx2-      | Lane 2 Tx Input I | 3 |
| 98  | GND       |                   |   |
| 99  | Tx3+      | Lane 3 Tx Input I | 3 |
| 100 | Tx3-      | Lane 3 Tx Input I | 3 |
| 101 | GND       |                   |   |
| 102 | N.C.      |                   |   |
| 103 | N.C.      |                   |   |
| 104 | GND       |                   |   |

**Notes:**

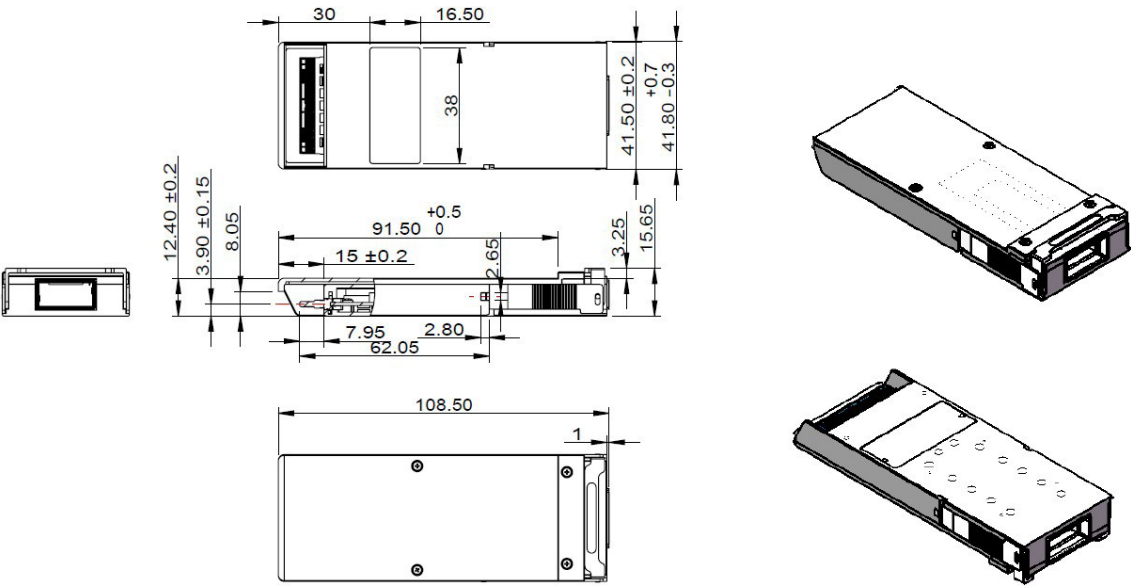
1. CML Output.
2. Reference Clock Input.
3. CML Input.
4. Ground connections are common for Tx and Rx.
5. Each connector contact is rated at 0.5A.
6. MDIO and MDC timing must comply with IEEE 802.3ae clause 45.3.
7. Converter will be MSA compliant when no signals are present on the vendor-specific pins.



Block Diagram



Mechanical Specifications



# About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box.

